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Evolution de la conception des « systèmes sur une puce » à l'ère des nanotechnologies

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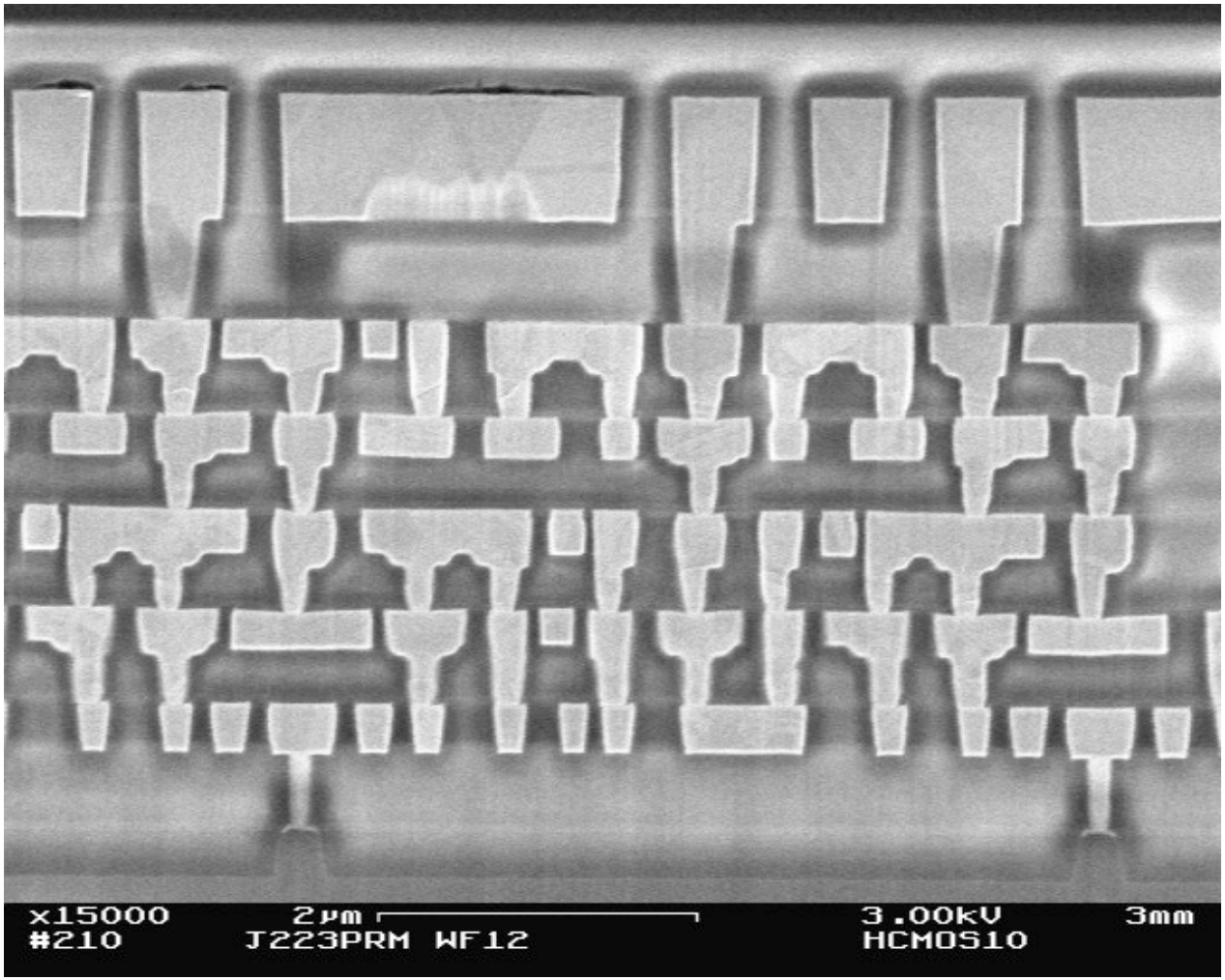
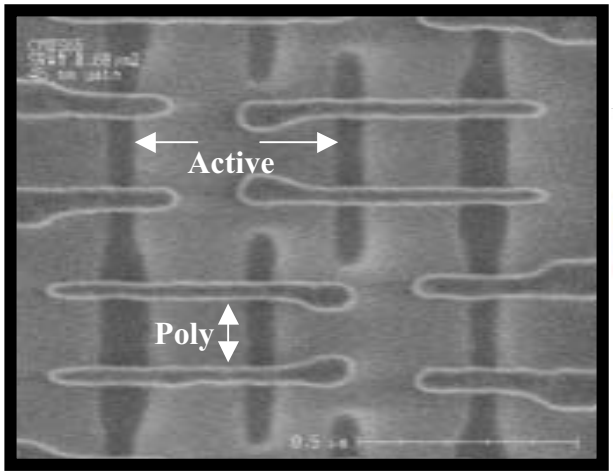
Agenda

- Technology Evolution
- New system requirements
- Hardware/Software co-design
- Design Complexity and manufacturing costs
- Concurrent hard/software design and validation
- Flexible and Reconfigurable SoC
- Conclusion

90nm full SiOC/Cu interconnect

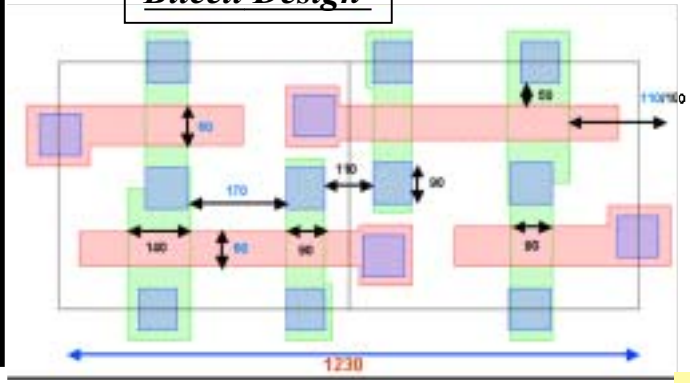


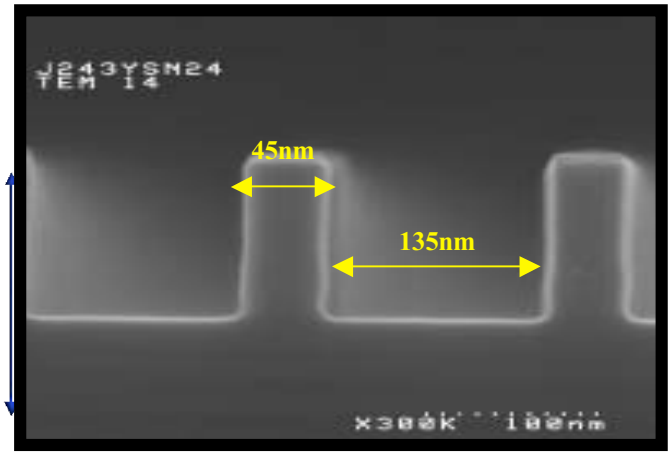
65nm Process Development – Crolles2



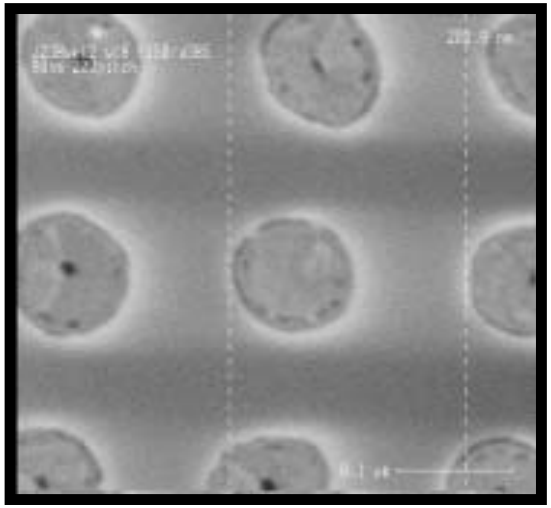
0.69um2 Bitcell

Bitcell Design

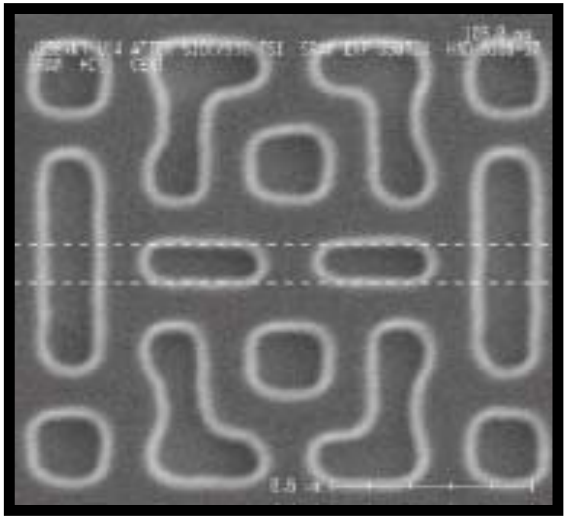




45nm Gate – (180nm Pitch)

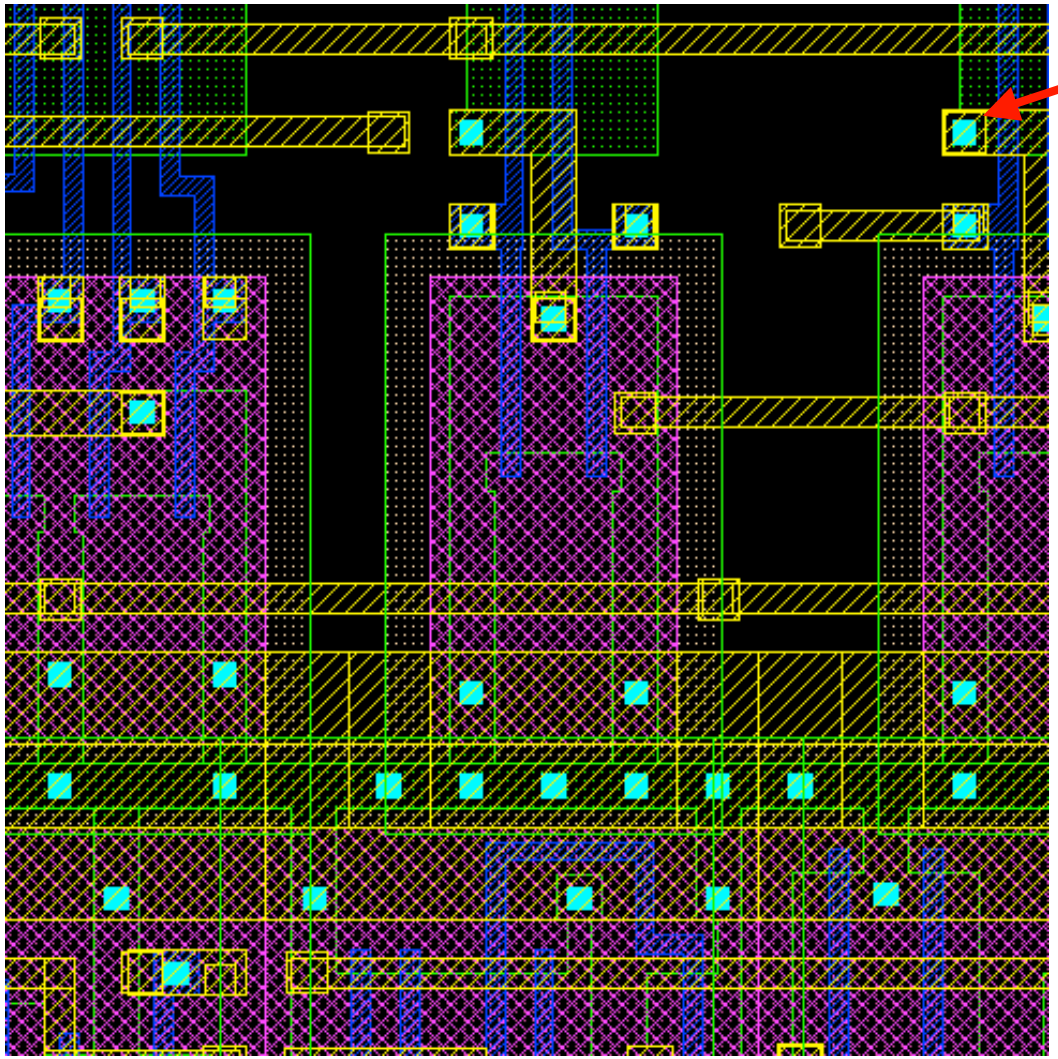


Contact polish – (200nm Pitch)



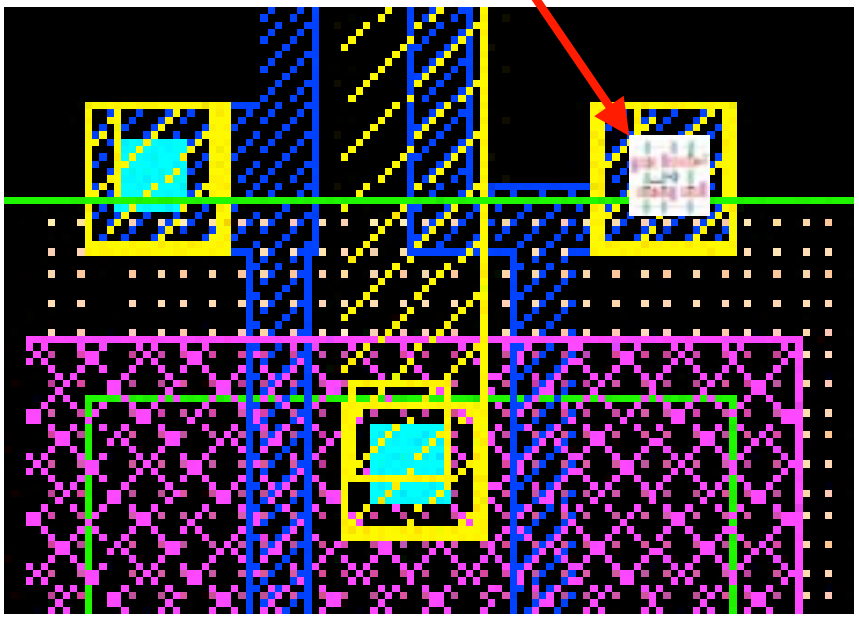
Line1 patterning – (200nm Pitch)

0.5um vs 65nm Design Rules

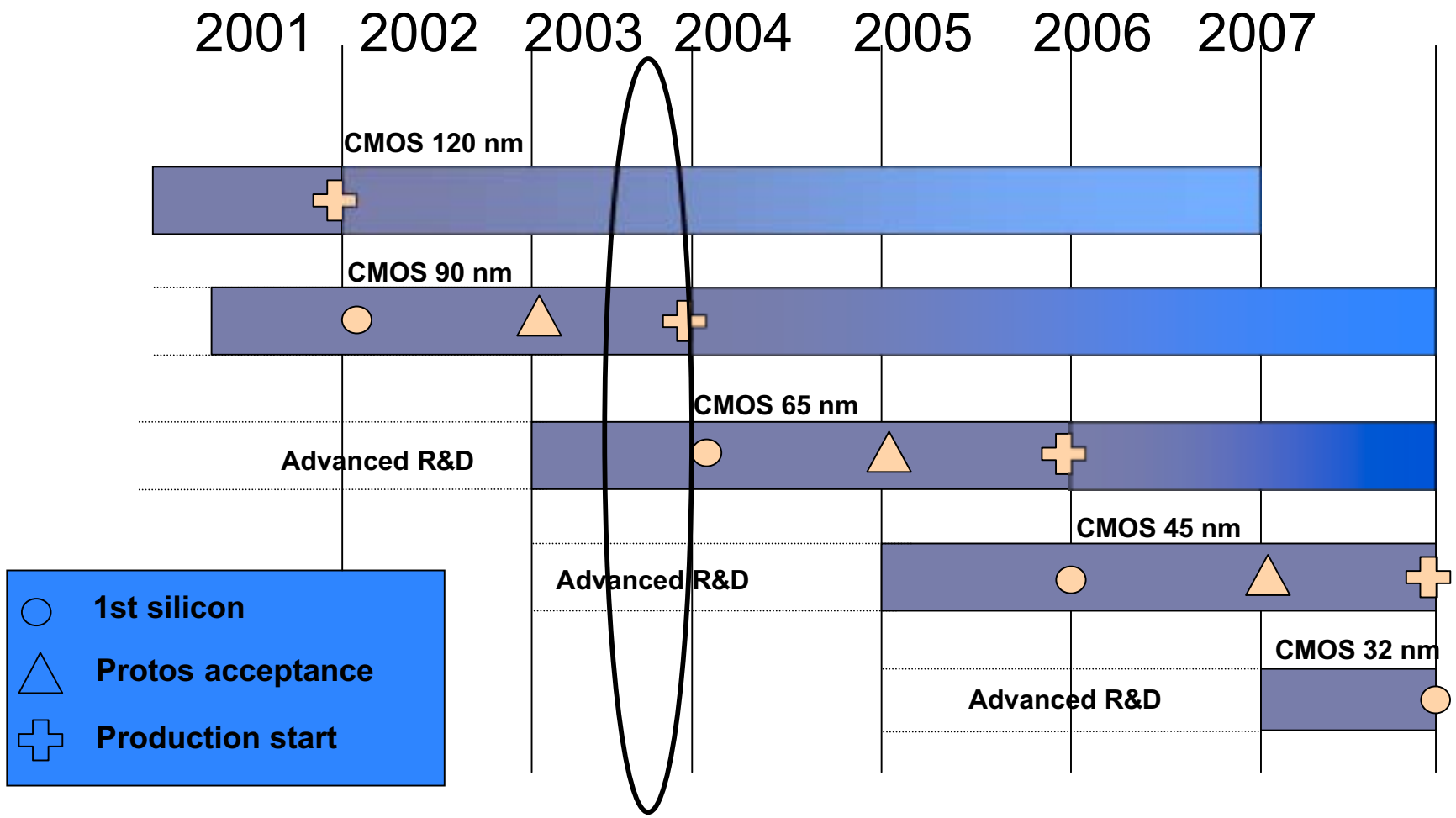


Contact in 0.5µm

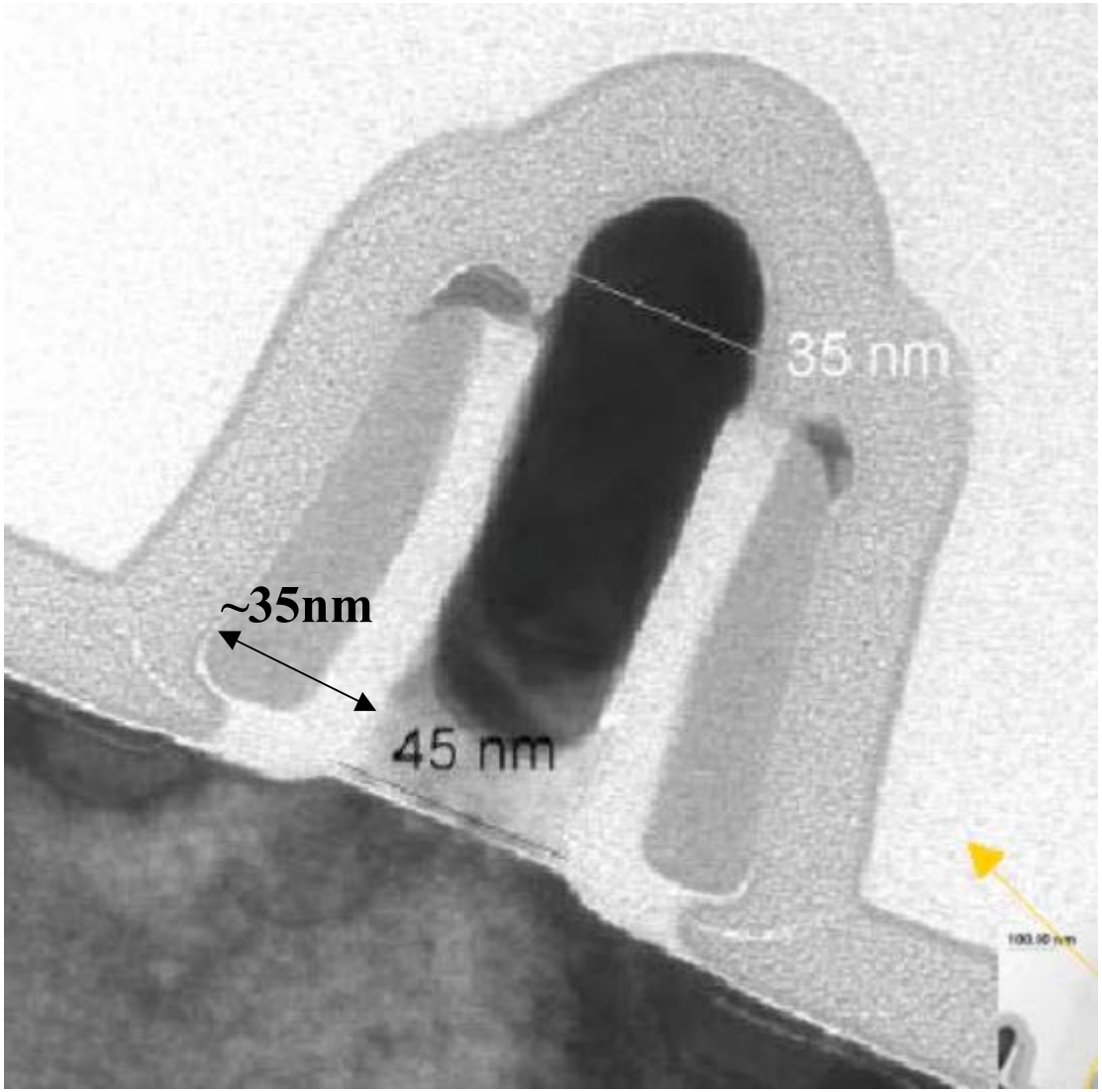
6-transistor SRAM cell in 65nm



CMOS Roadmap: from R&D to production



45nm gate for GP device without Offset spacers



Courtesy of F. Arnaud

2 opposite requirements for the future

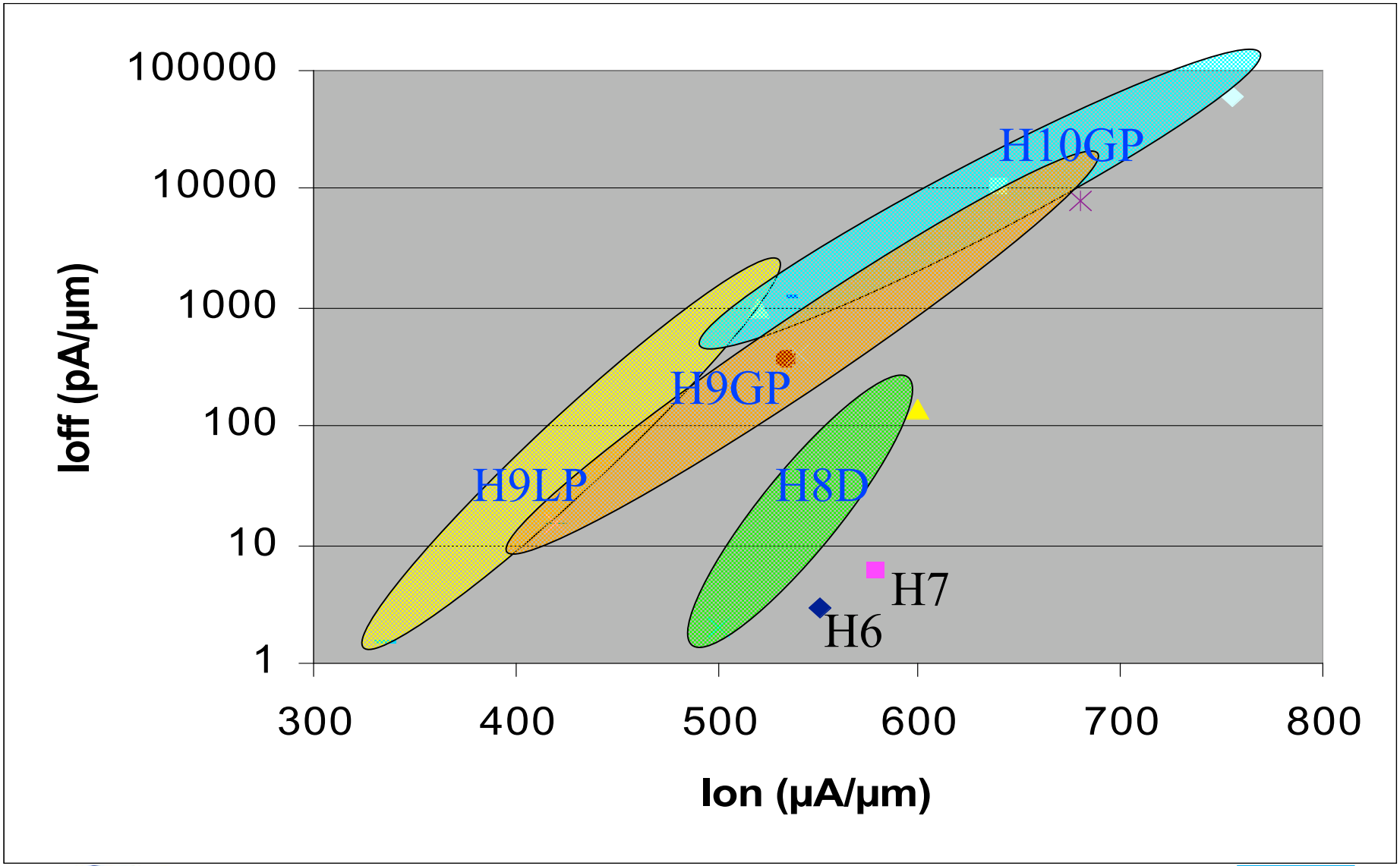
- Increase processing power (GOPS):
  - Video, Audio, Graphics, Communications:
    - **High performance dedicated processors**
    - **A lot of embedded memories**
  - Replace Analog by Digital (e.g. digital Radio)

- Reduce power consumption (Watt/Op):
  - Dynamic power = CV^2f
    - **C: Need SOI-like junctions and LowK dielectrics**
    - **V: decrease VDD to the minimum to achieve Frequency f**
    - **F: keep Frequency pretty low, use parallelism**
  - Static power = as low as possible

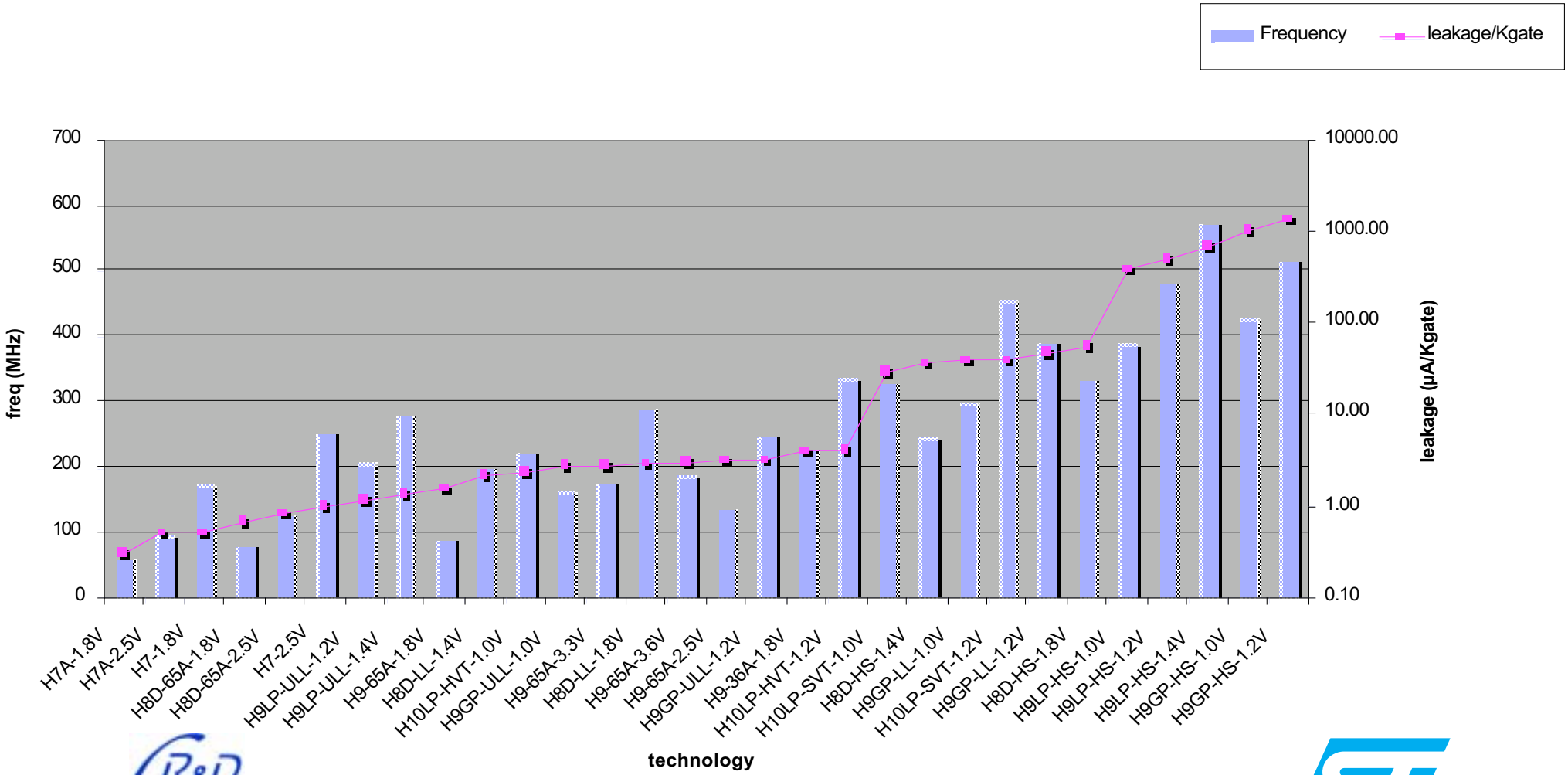
Static versus Dynamic Power

- Dynamic Power per Chip is rather stable due to system limitation: mechanical / battery
- Dynamic Power is under control:
  - VDD is decreasing (slowly)
  - Power management is in practice (clock gating, power shut down, …)
- Static Power is not under control: natural leakage of transistor multiplied by 10 every 2 years:
  - Power shut down is the best way to cut leakage
  - Very low voltage retention or zero leakage Non Volatile memories are potential solutions
- Static Power is becoming as big as Dynamic Power at high temperature (wasted power, no solution)

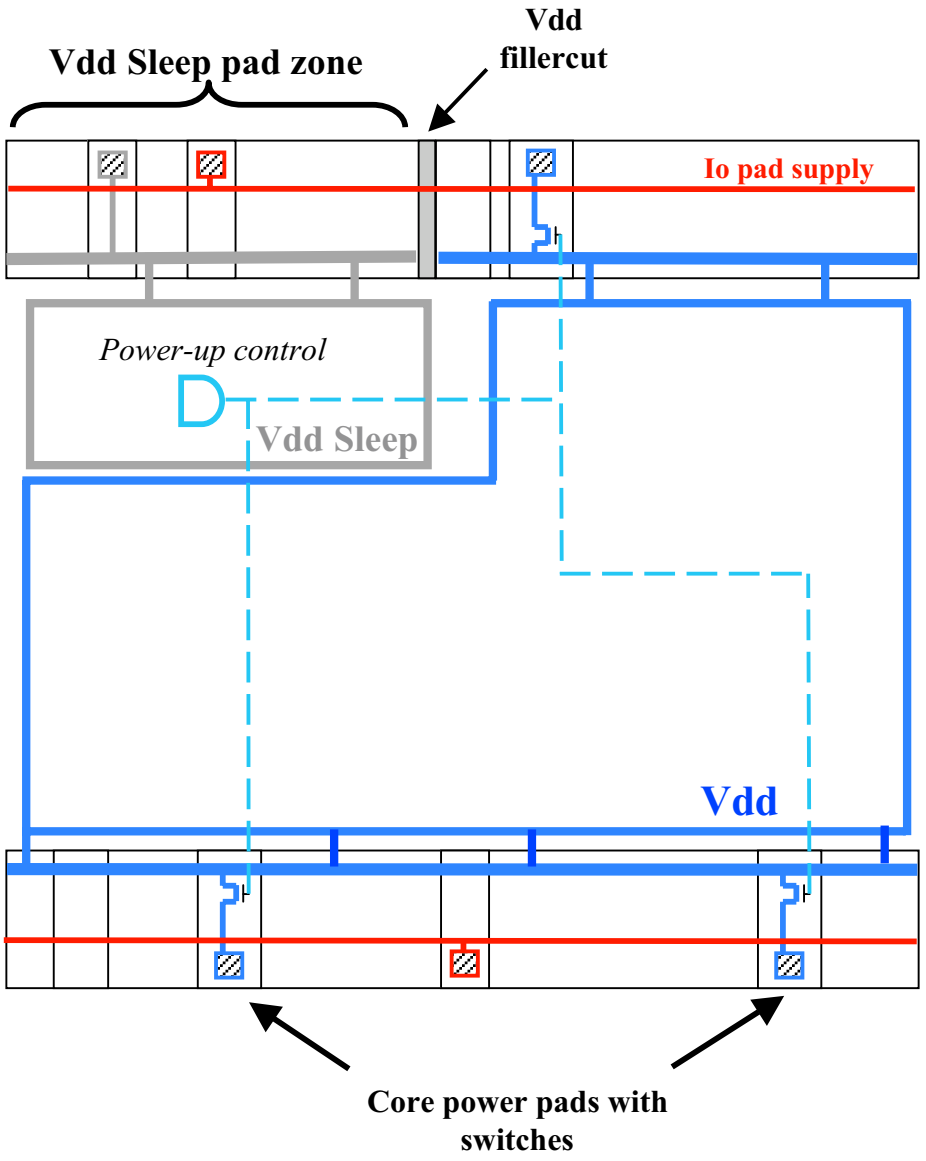
Nmos Ion/Ioff evolution

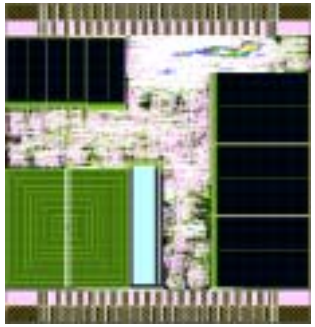


SoC Frequency & Leakage evolution from 250nm to 90nm



Low-Power techniques for wireless



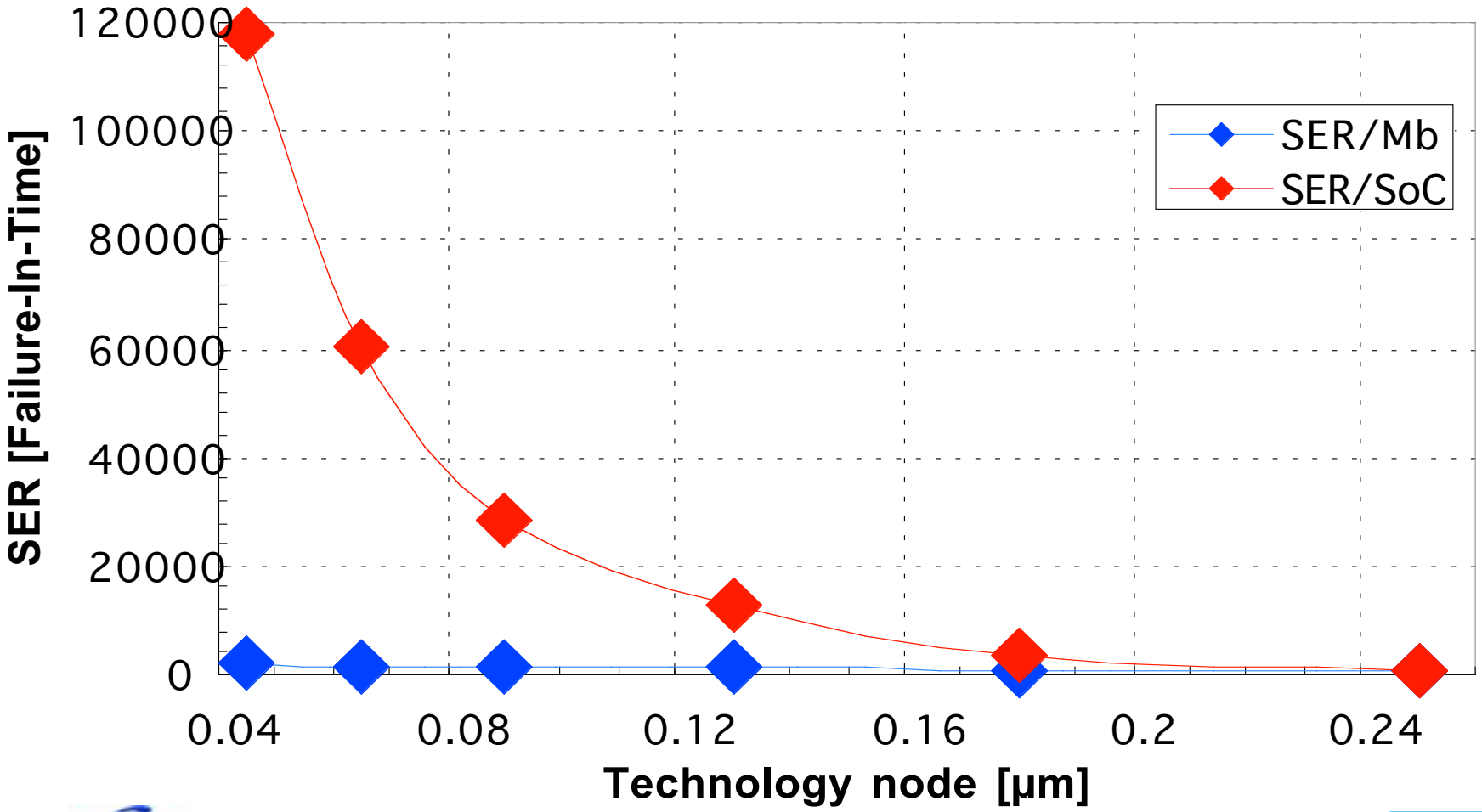


- Two supply zones: Vdd and VddSleep.
- Specific rules at RTL for boundary between Vdd and VddSleep areas
- Gnd is common for all cells.
- Pads are always powered.
- 3 power pads with embedded switches

SoC SER increase with technology down scaling

The percentage of SRAM per System on Chip (SoC) is derived from ITRS 2002

Same trend for total Standby Power !



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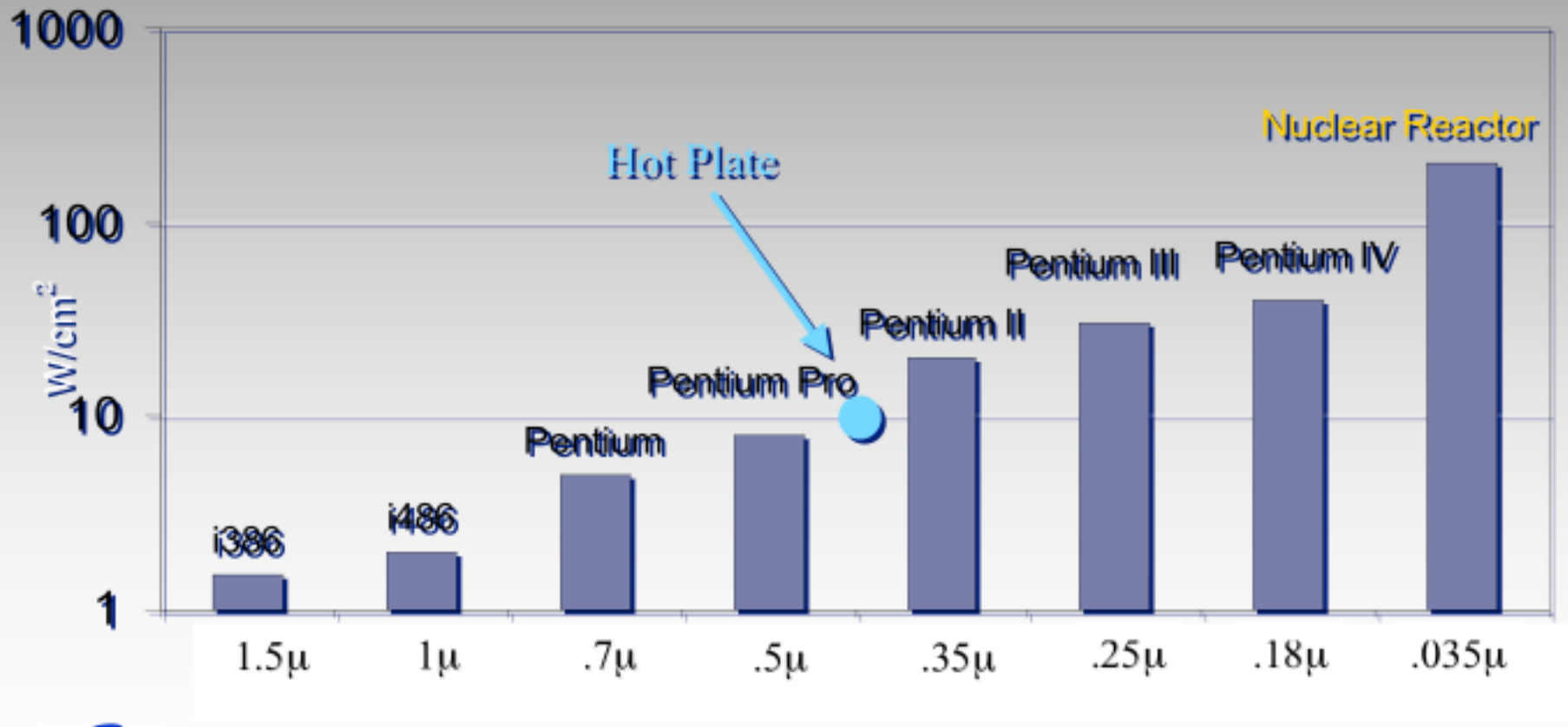
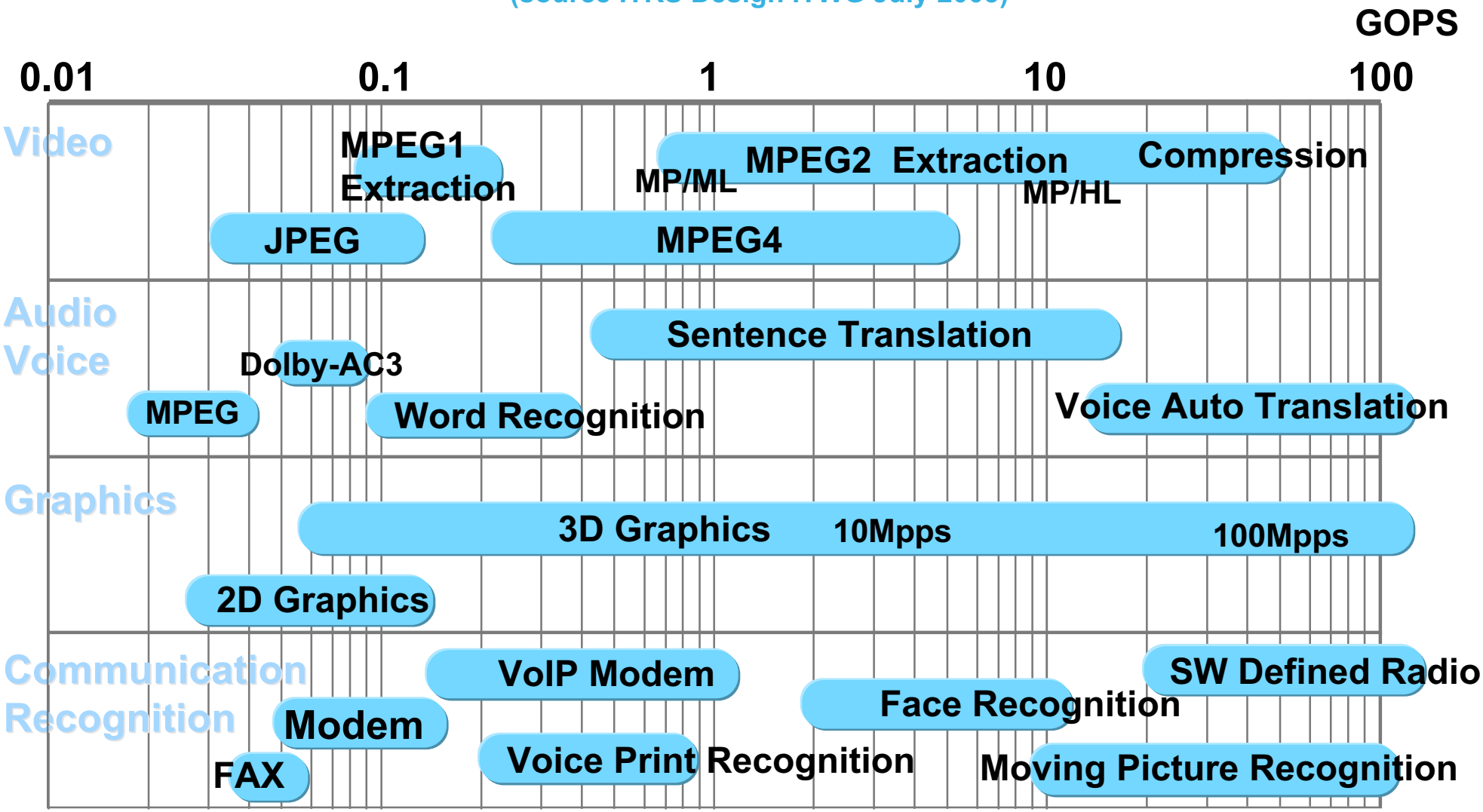
Power Density in Microprocessors



Fred Pollack, Intel

Required Performance for Multi-Media Processing

(source ITRS Design ITWG July 2003)



GOPS: Giga Operations Per Second

PDA Model Characteristics
(source ITRS Design ITWG July 2003)

Process Technology (nm)	130	90	65	45	32	22
Operation Voltage (V)	1.2	1	0.8	0.6	0.5	0.4
Clock Frequency (MHz)	150	300	450	600	900	1200
Application (MAX performance required)	Still Image Processing	Real Time Video Codec (MPEG4/CIF)		Real Time Interpretation		
Application (Others)	Web Browser Electric Mailer Scheduler	TV Telephone (1:1) Voice Recognition (Input) Authentication (Crypto Engine)		TV Telephone (>3:1) Voice Recognition (Operation)		
Processing Performance (GOPS)	0.3	2	14	77	461	2458
Parallelism Factor	1	4	4	4	4	4
Communication Speed (Kbps)	64	384	2304	13824	82944	497664
Power Consumption (MOPS/mW)	3	20	140	770	4160	24580
Peak Power Consumption (mW) (Requirement)	100	100	100	100	100	100
Standby power consumption (mW) (Requirement)	2	2	2	2	2	2
Battery Wh/Kg	120	200		400		

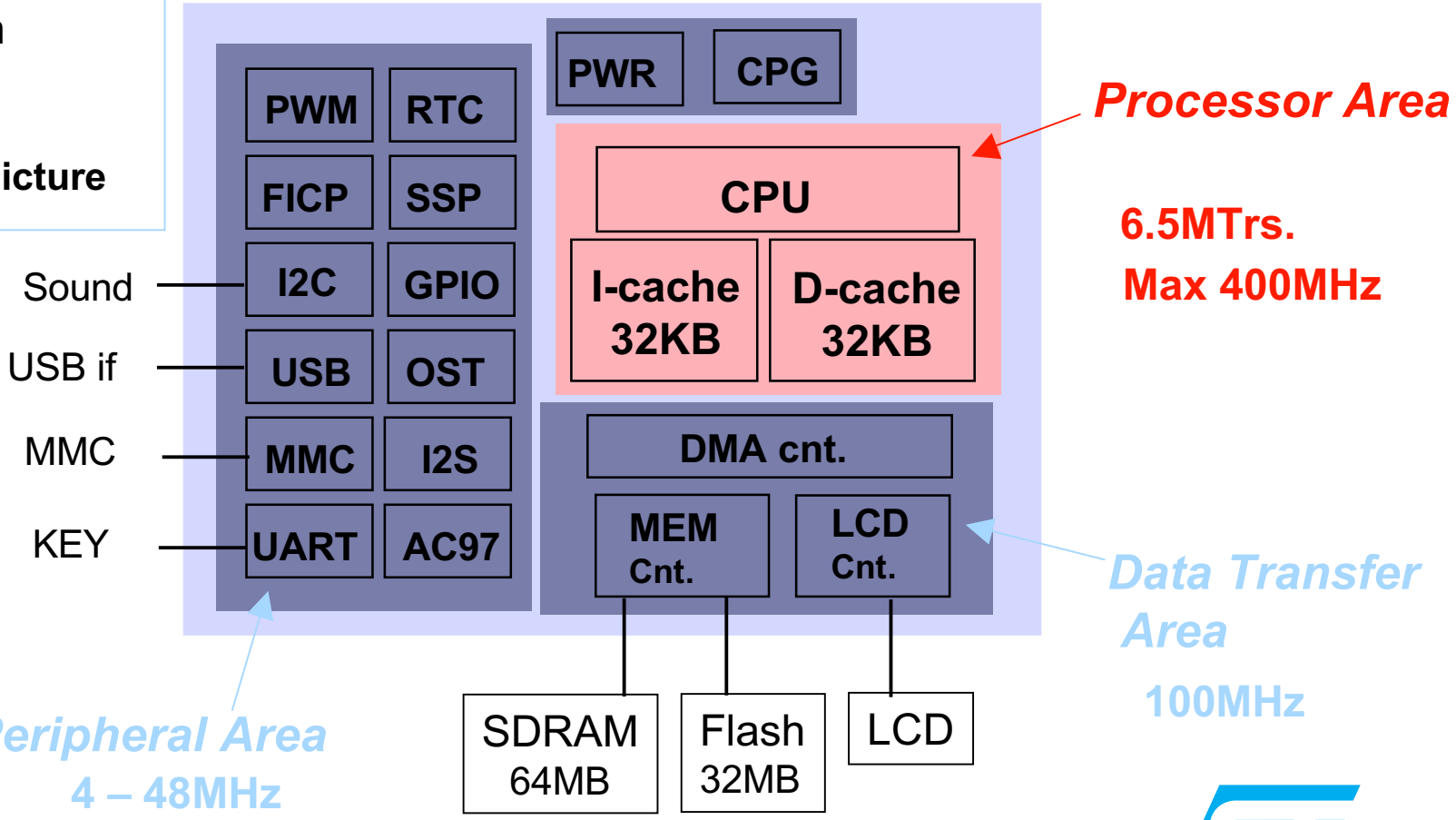
An Example of SoC for PDA

(source ITRS Design ITWG July 2003)

Specification

-Available Time
6-10Hr
-MM Application
MP3
JPEG
Simple Moving Picture

0.18um/400MHz/470mW (typ)



Processor Area

6.5MTrs.
Max 400MHz

Data Transfer Area

100MHz

Peripheral Area
4 – 48MHz

An Example of SoC for Mobile Phone

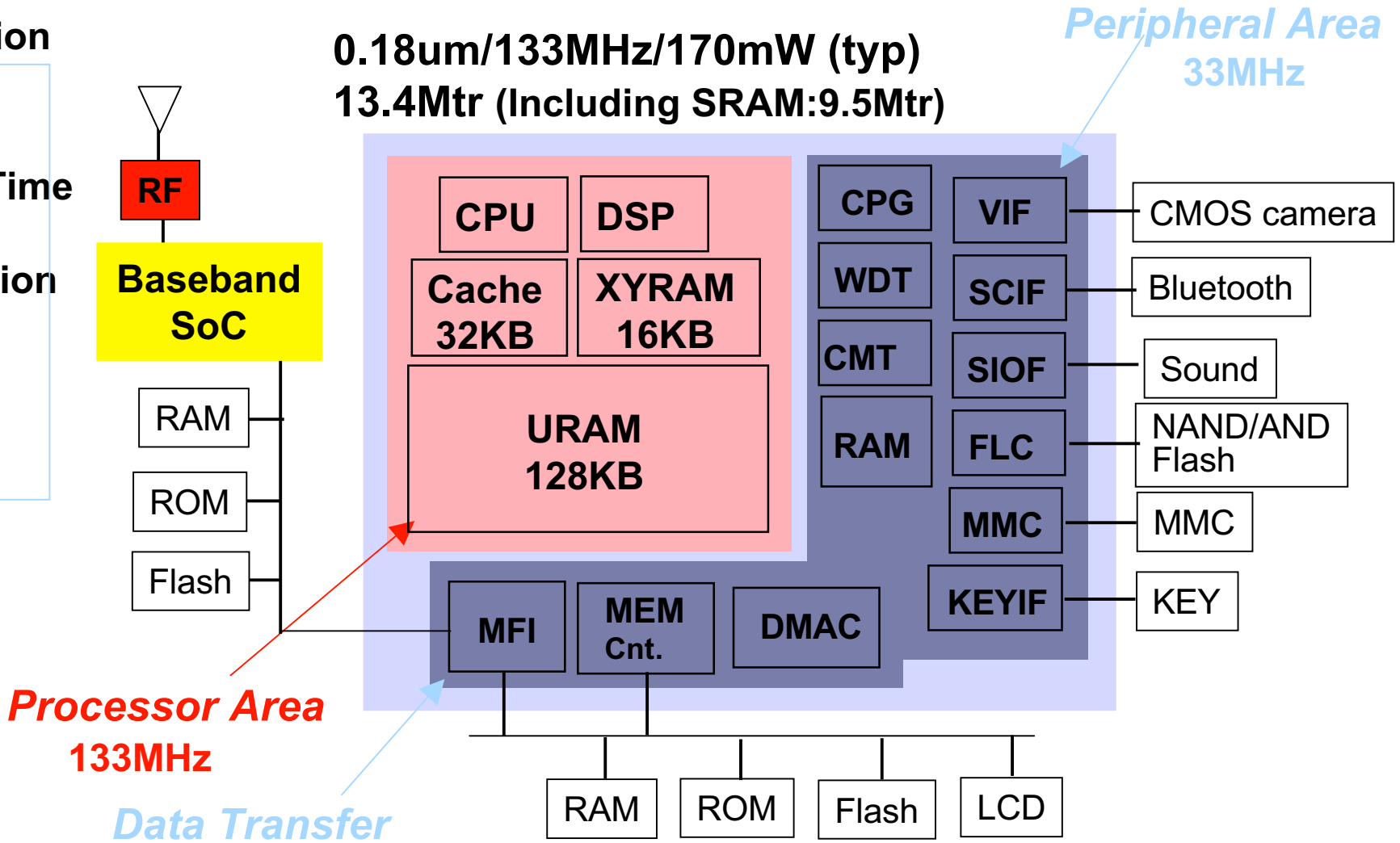
(source ITRS Design ITWG July 2003)

Specification

- -Talk Time
  - 140min.
- -Standby Time
  - 200Hr
- -MM Function
  - MP3
  - JPEG
  - MPEG4
  - Java

0.18um/133MHz/170mW (typ)

13.4Mtr (Including SRAM:9.5Mtr)

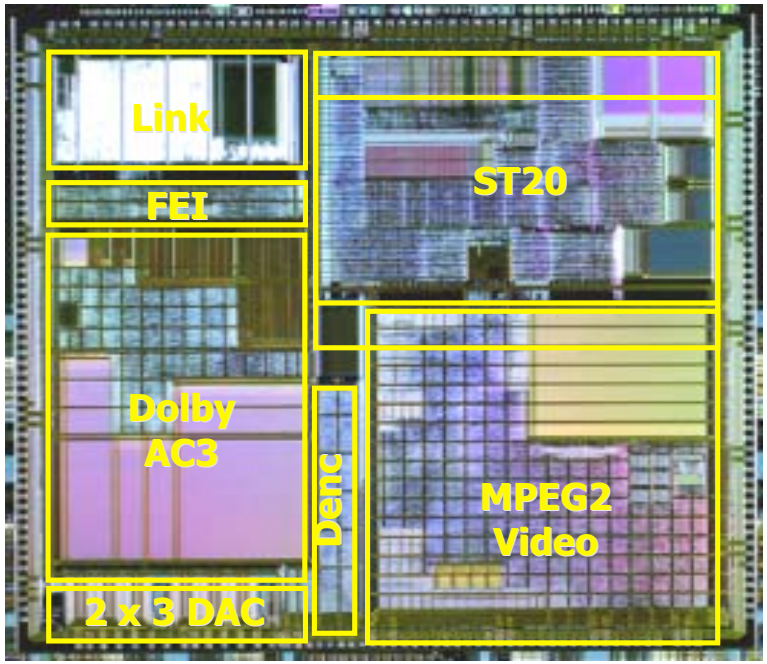


SoC at the heart of conflicting trends

Time-to-market:

Process roadmap acceleration

Consumerization of electronic devices



Complex systems:

- uCs, DSPs HW/SW
- SW protocol stacks
- RTOS,s
- Digital/Analog IPs
- On-Chip busses
- Process options explosion (analog, RF, imagers, …)

Deep sub micron effects:

- crosstalk
- electro migration
- wire delays, on-chip-variation
- mask costs (OPC, PSM)
- copper wires

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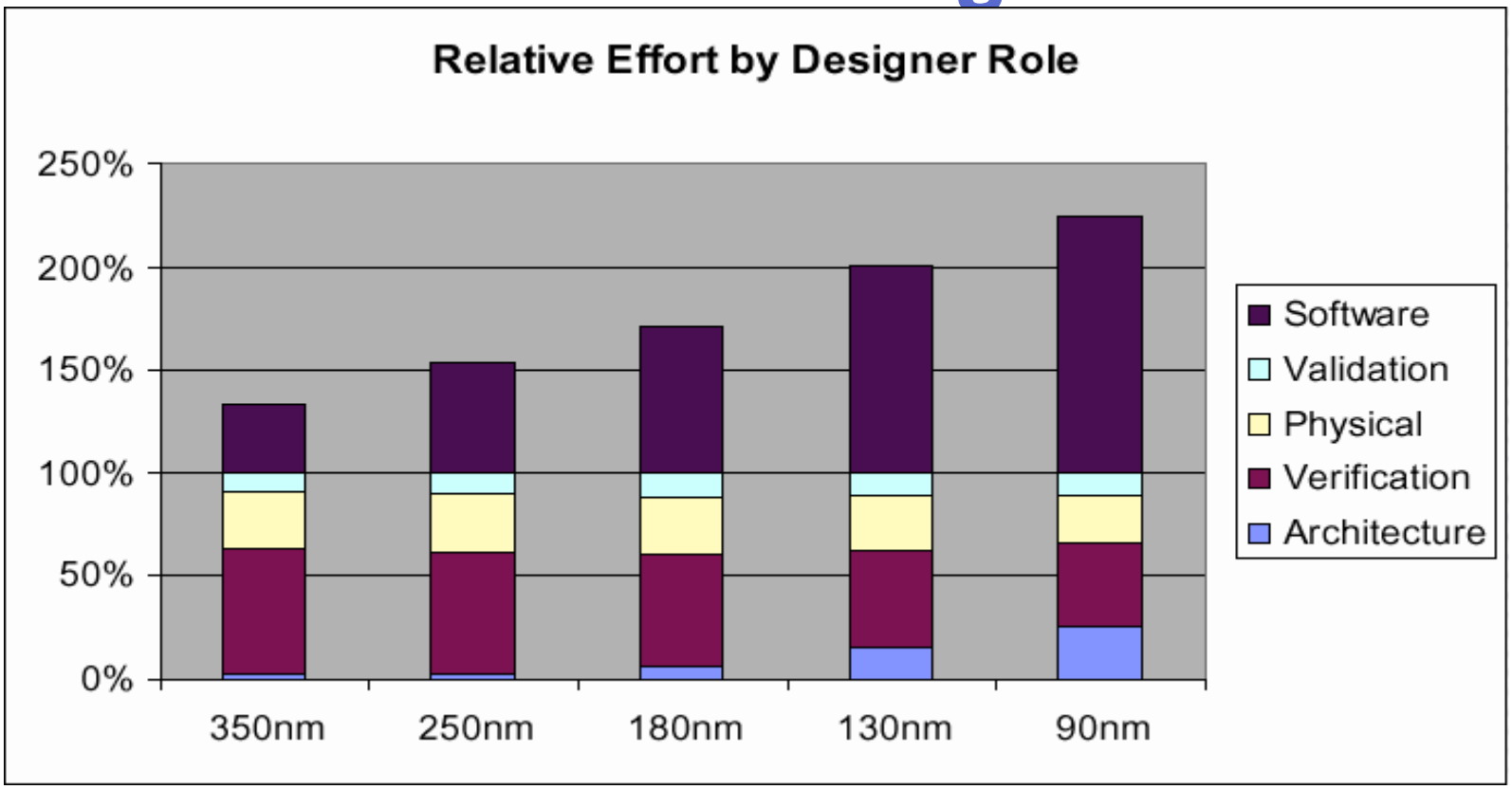
SoC Design + Rising Complexity = New Challenges

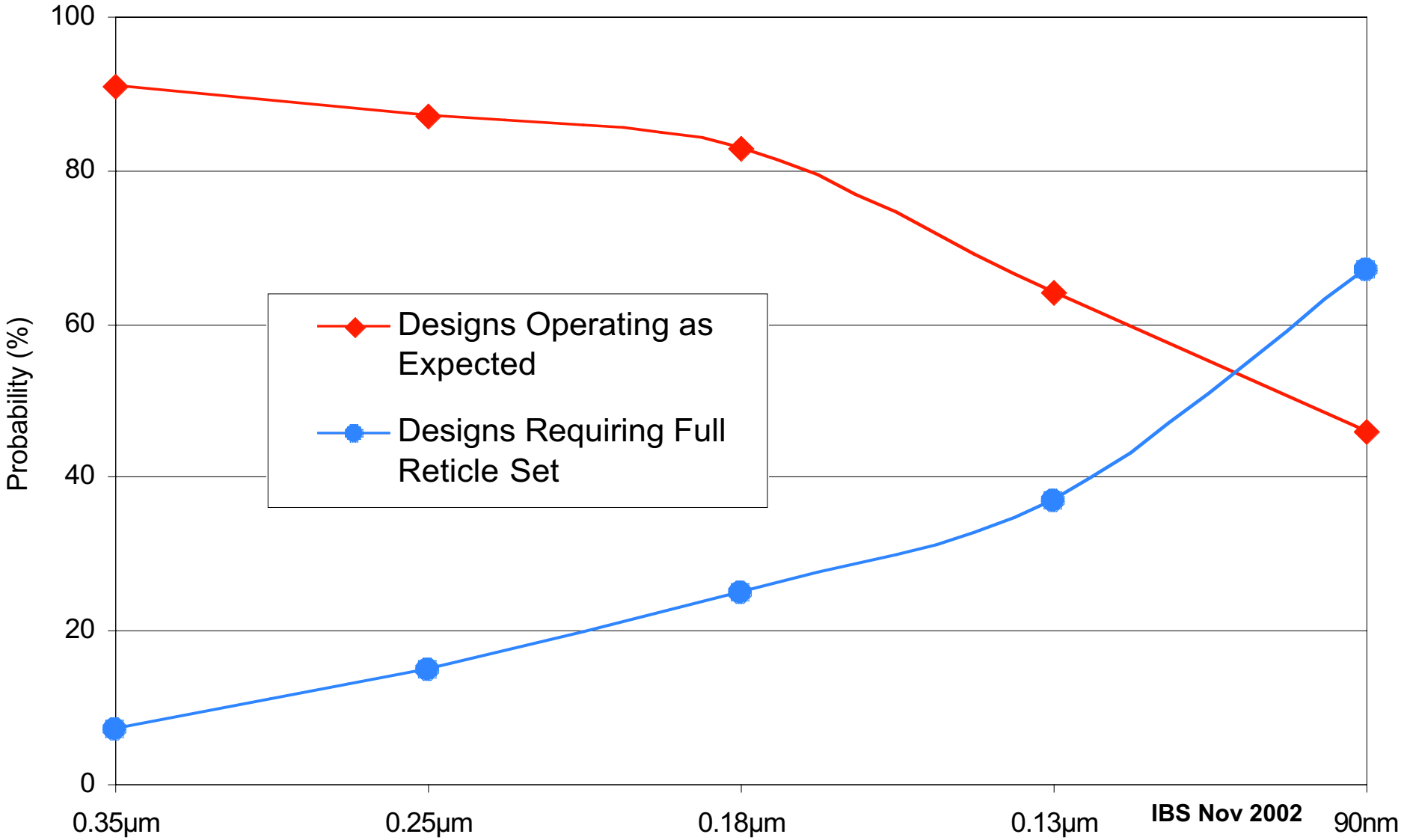


IBS Nov 2002

* Architecture effort overtakes physical design at 90nm

* Software costs overtake total hardware costs at 130nm

PROBABILITY OF DESIGNS OPERATING AS EXPECTED



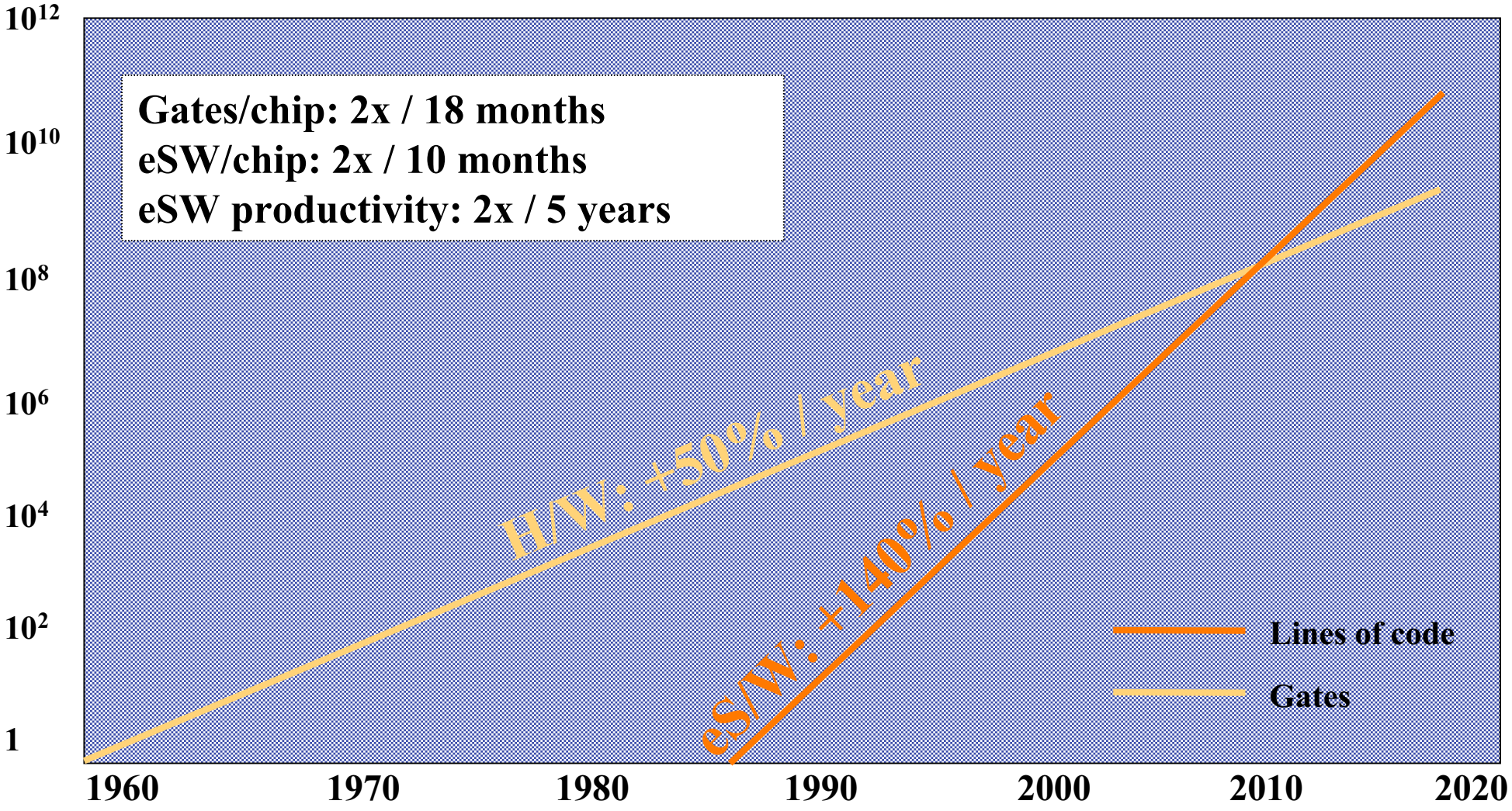
Key Trends: ASICs down, Multi-processors & FPGAs up

- ASIC/ASSP ratio: 80/20 in 2000, 50/50 in 2003
- Telecom company trends
  - In-house ASIC design way down
  - Replace by commercial off-the-shelf, programmable ASSP
  - High-end NPU's used in non-NPU applications
- Number of embedded processors in SoC rising:
  - ST: recordable DVD 5
  - Hughes: set-top box 7
  - ST: HDTV platform 8
  - Latest mobile handsets 10
  - NEC: Image processor 128
  - In-house NPU >150

Key Trends: Embedded S/W content in SoC is way up

- eS/W: Current application complexity
  - Set-top box: >1 million lines of code
  - Digital audio processing: >1 million lines of code
  - Recordable DVD: Over 100 person-years effort
  - Hard-disk drive: eS/W represents 100 person-years effort
- In multimedia systems
  - S/W cost (licenses, royalties) 6X larger than H/W chip cost
  - eS/W uses 50% to 80% of design resources
- eS/W has become an essential part of SoC products
- Software reuse essential now
- Software architecture becoming important
- Memory now dominating die area

S/W and H/W Complexity Factors



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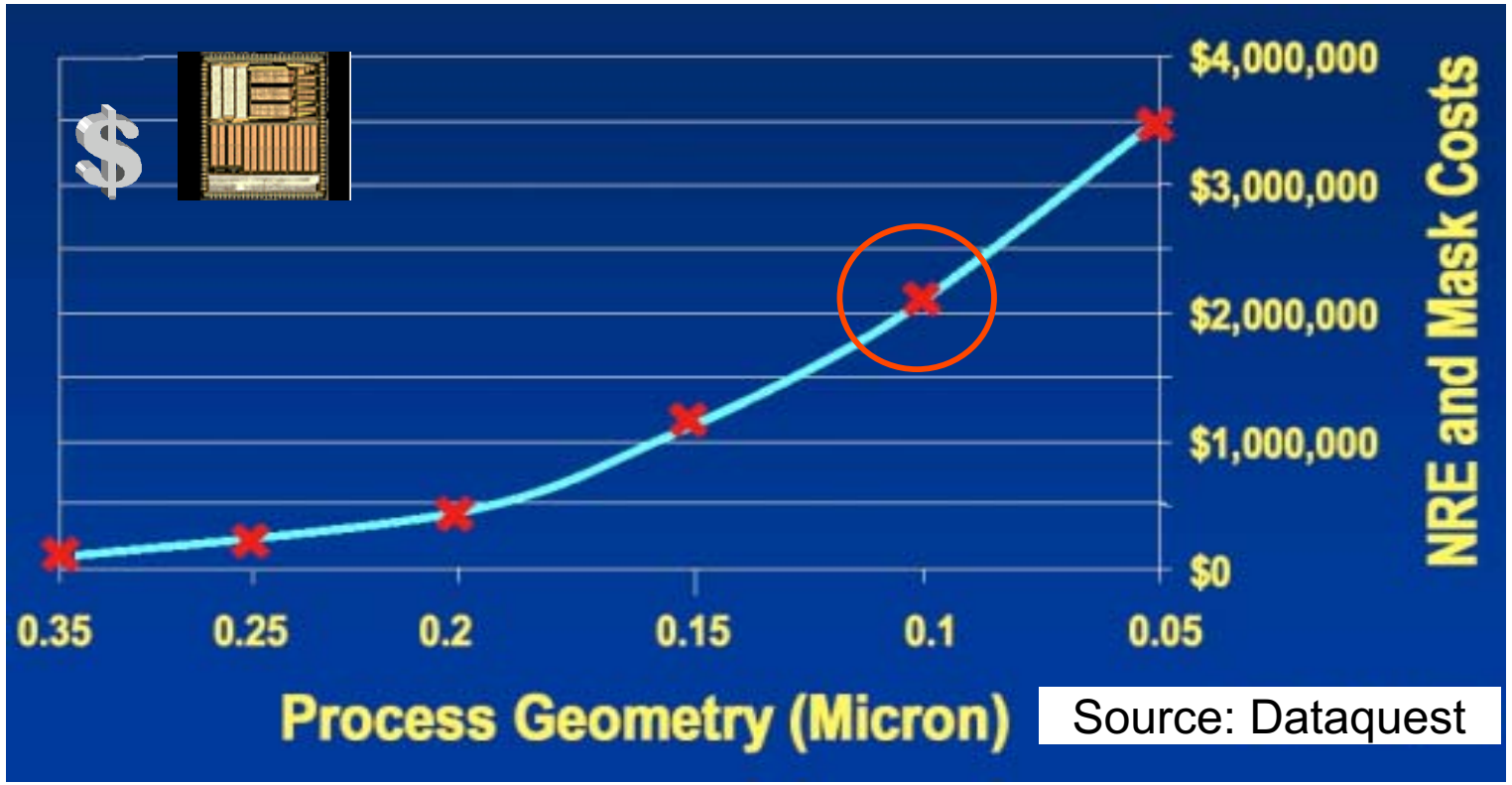
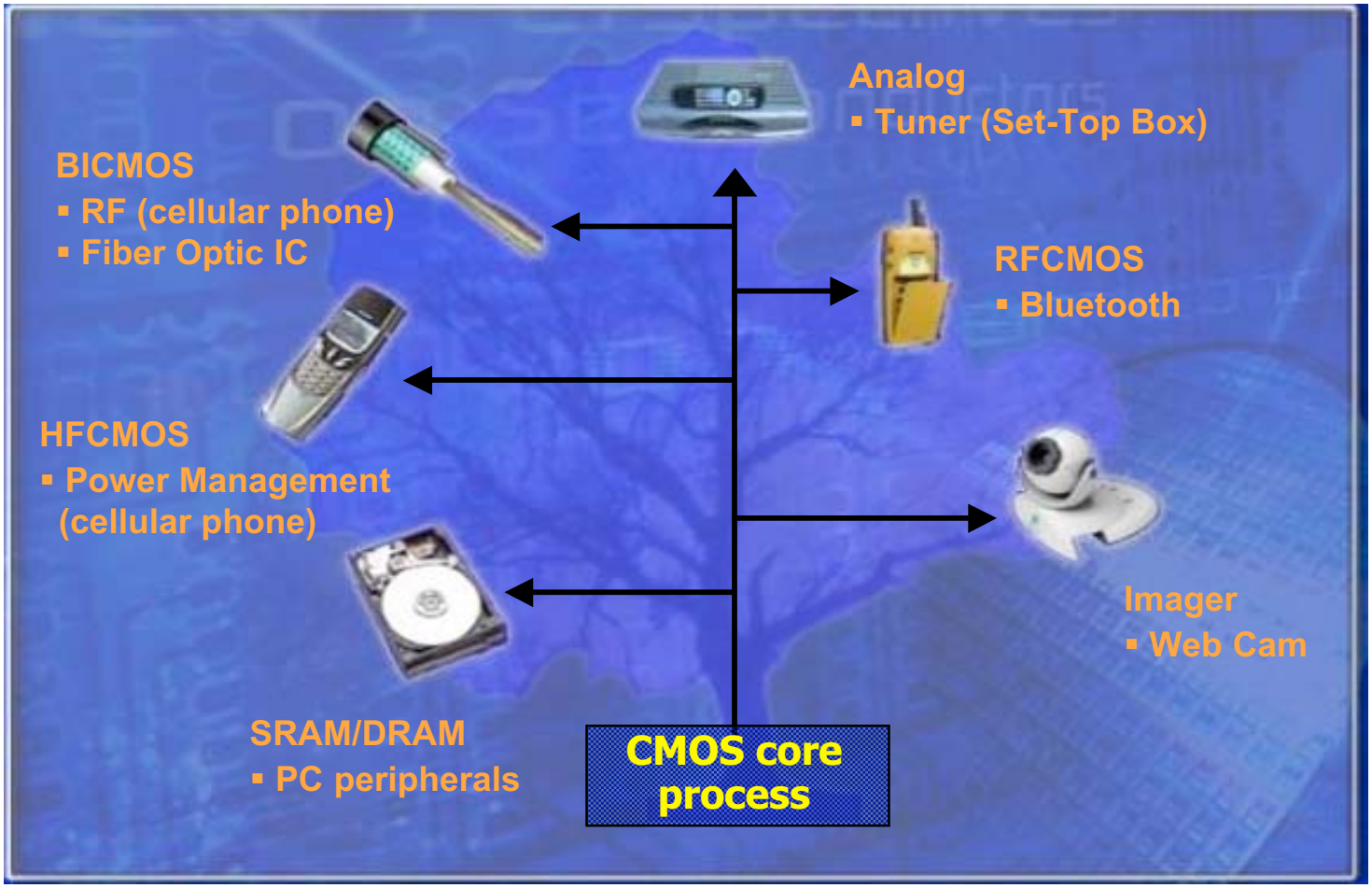
SoC Economic Trends: Mask NRE

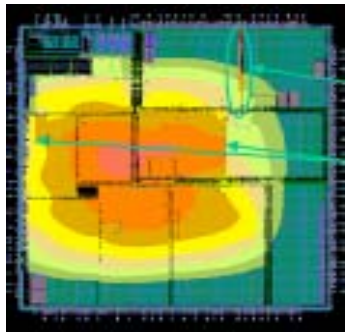


– For $5 ASP with 25% profit margin:
  Need to sell over 1.6M parts to break even

Extending Core CMOS for SOC

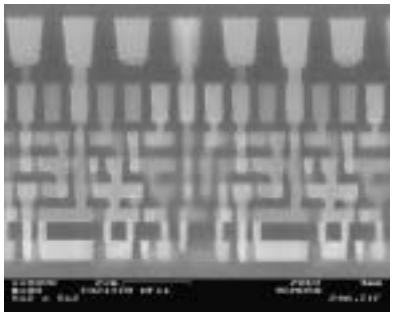


Deep Submicrons Effects modeled in 0.13um

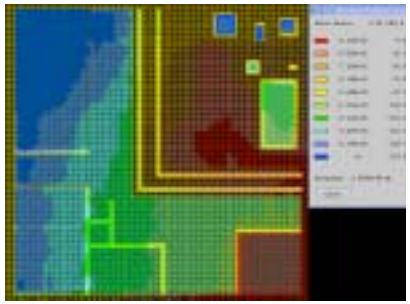


Voltage Drop & EMG

Copper Routing



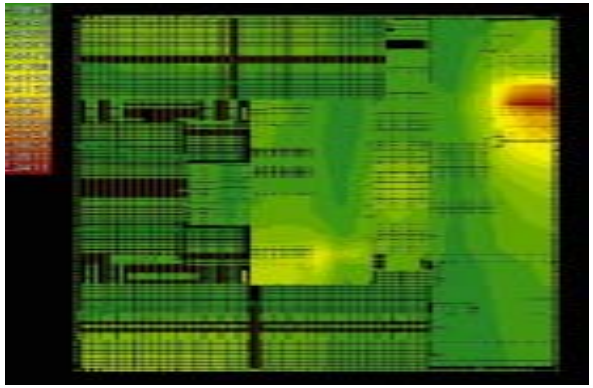
Cross Talk effects

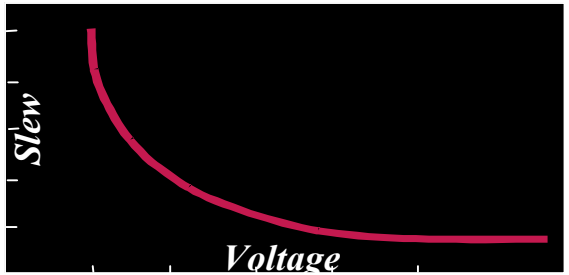


Substrate Noise

New Timing Effects (90nm)

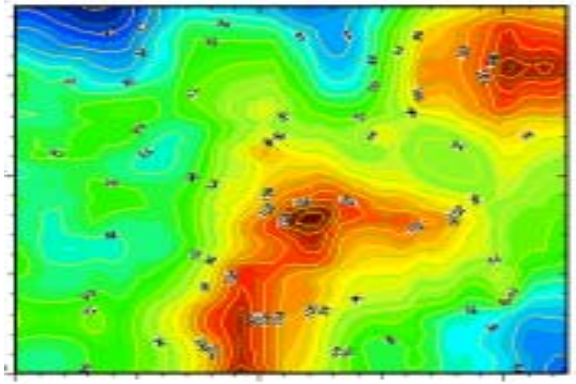
Voltage on-chip-variations

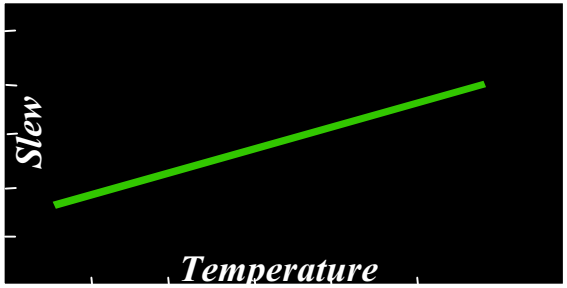




5% voltage change →
15% change in slew

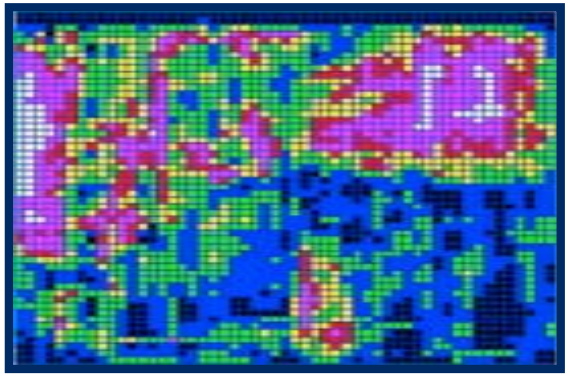
Temperature Map

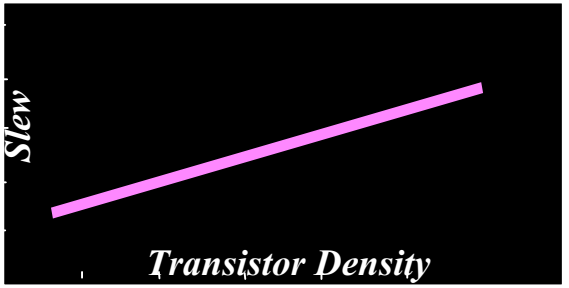




30° C change →
7% change in delay & slew

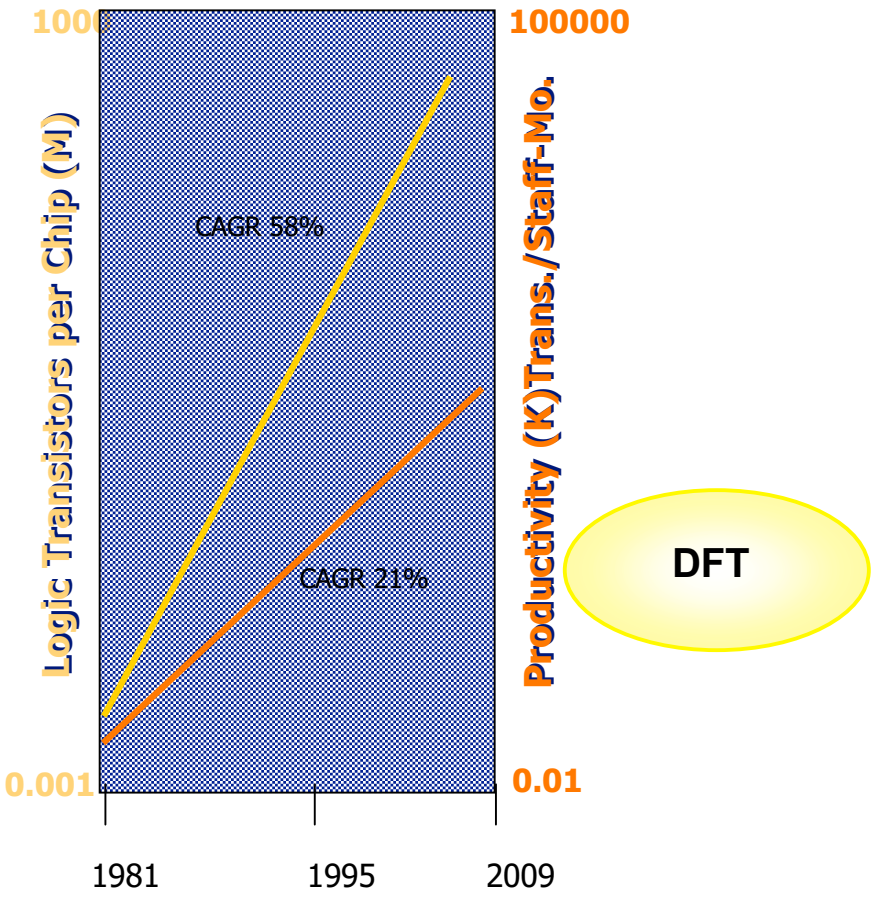
Transistor Density





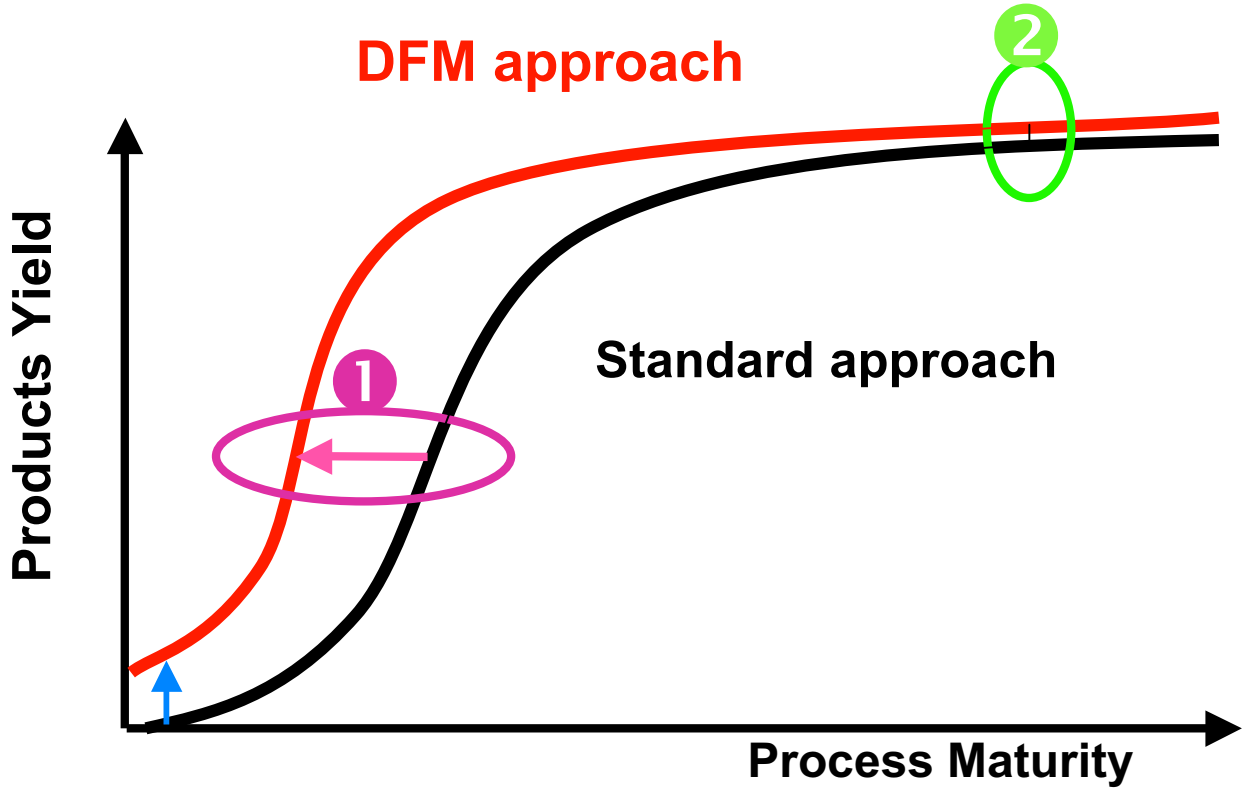
50% density change →
15% change in slew

Design For Test



- Memory generators: eSRAM, eDRAM eROM, eNVM
  - Include BIST generation
  - Redundancy mandatory above 1Mbit
- Logic
  - Scan / ATPG today
  - Commercial tools to reduce test times by 10X
  - Implementing IEEE P1500 for core-based test
- Design-for-Manufacturing
  - Yield-improving design guidelines under definition

Design For Manufacturability Gains



2 Yield gain for **mature** process (3 to 5%)

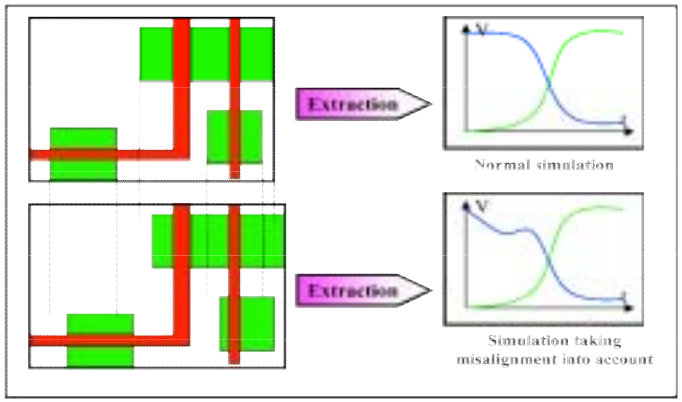
3 Robustness increase (versus design marginalities)

1 **Acceleration** for **ramp-up** process (~months)

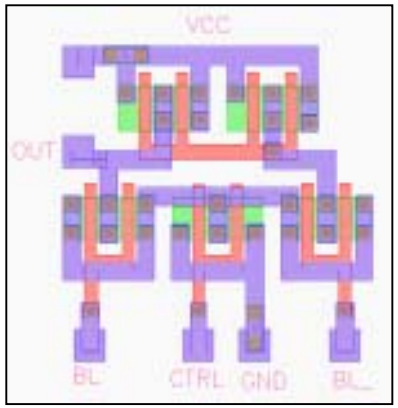
4 Reliability improvement

Design For Manufacturability

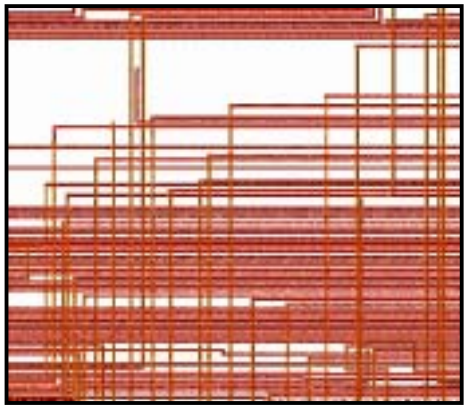
Misalignment impact



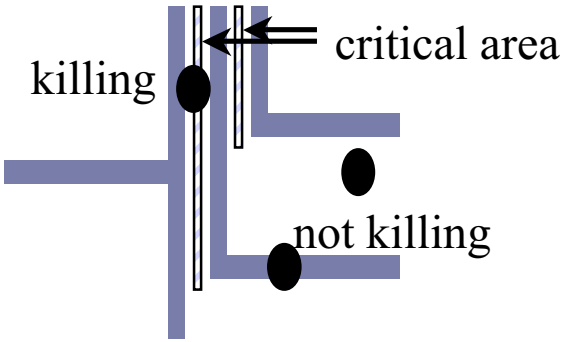
Matching robustness

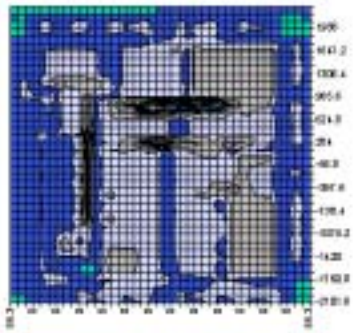


Wire spreading

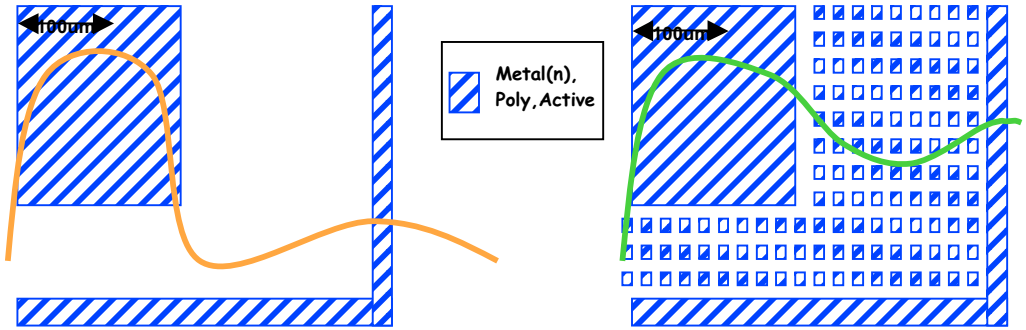


Critical area computation



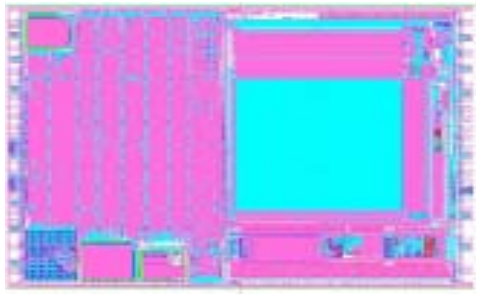


Tiling – densities for CMP



SoC,s with CMOS-Imager process

- **For mobile phone applications:**
  - ✓ **ZS450**: CIF format (~100000 pixels)

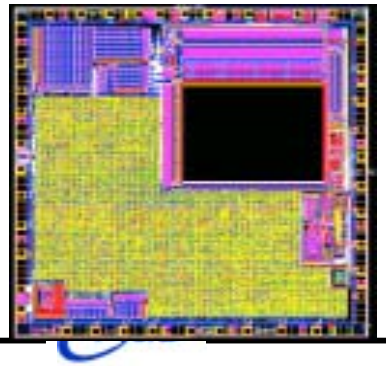


Area
24.0 mm_

  - ✓ **ZS550**: VGA format (~300000 pixels)

Area
39.6 mm_

- **For webcam applications:**
  - ✓ **ZS422**: QVGA format (~75000 pixels)
    => audio/video/video processing (SOC)

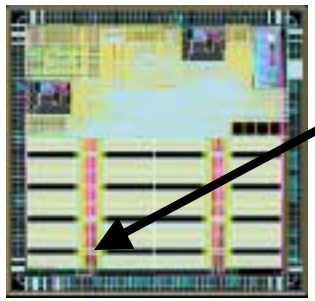


Area
24.1 mm_

Production 0.18um SoC,s with eDRAM

Low-End Printer

(20mm_)

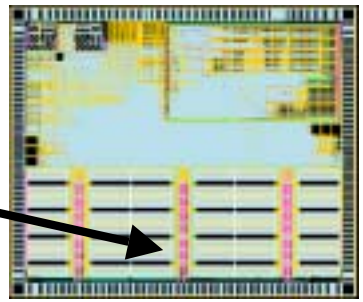


4 Mbits eDRAM

Includes ARM micro

High-End Printer

(34 mm_)



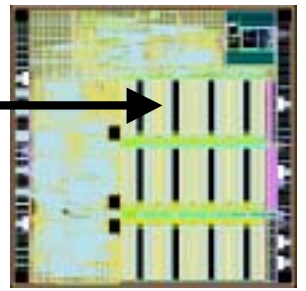
6 Mbits eDRAM

Includes ARM micro

Camera for cell phone

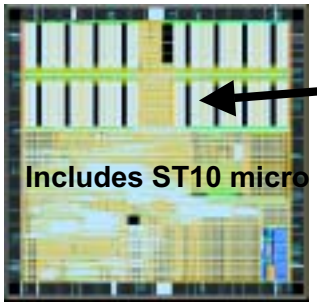
(15 mm_)

3 Mbits eDRAM



Disk Controller

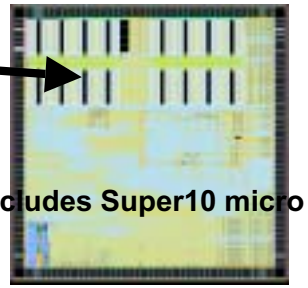
(26 mm_)



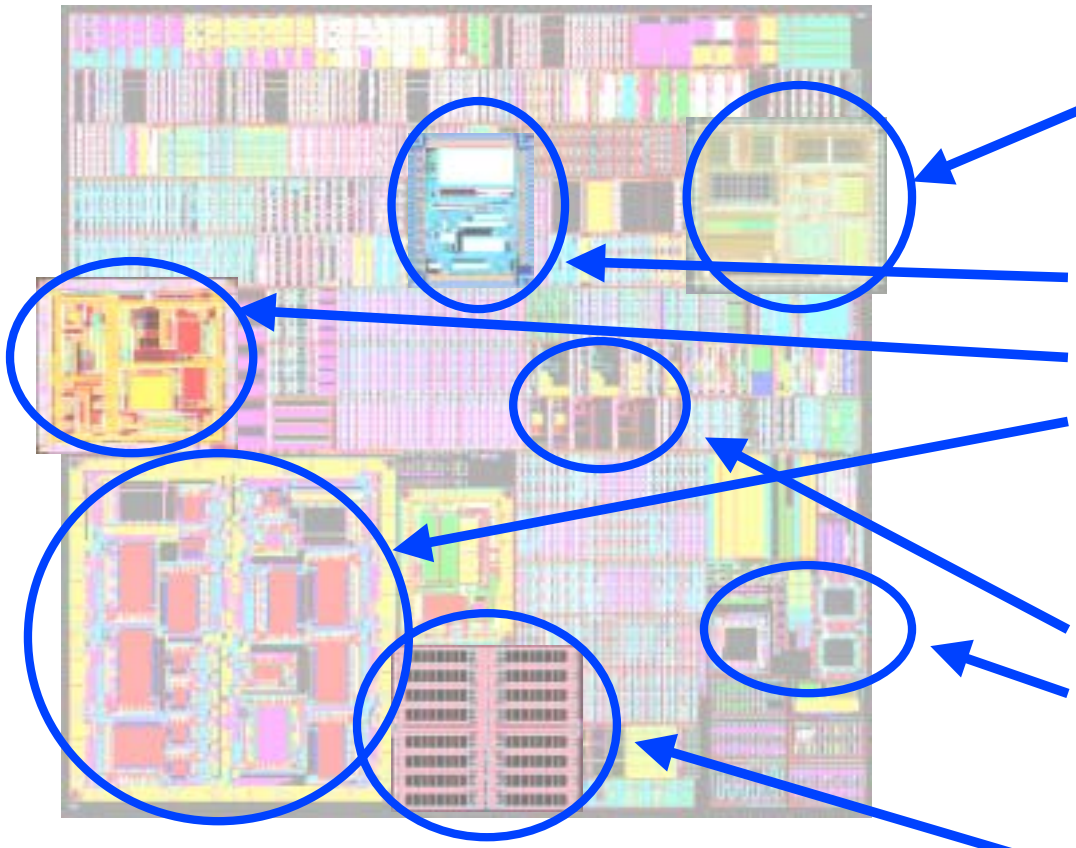
4 Mbits eDRAM

DVD recorder

(34 mm_)



IP & design validation effort
case study – 90nm test masks



- ASIC prototype
  - 30 Mtrans
  - SRAMs/ROM, PLL, IOs
  - Std cells IPs
- ROM compiler validation
- SRAM compilers
- SRAM bitcells qualification
  - 17.5 Mbits
- Analog/RF IPs
- IOs & fuse prototypes
- eDRAM macrocell
  - 12 Mbits

Emb.memory offering expanding

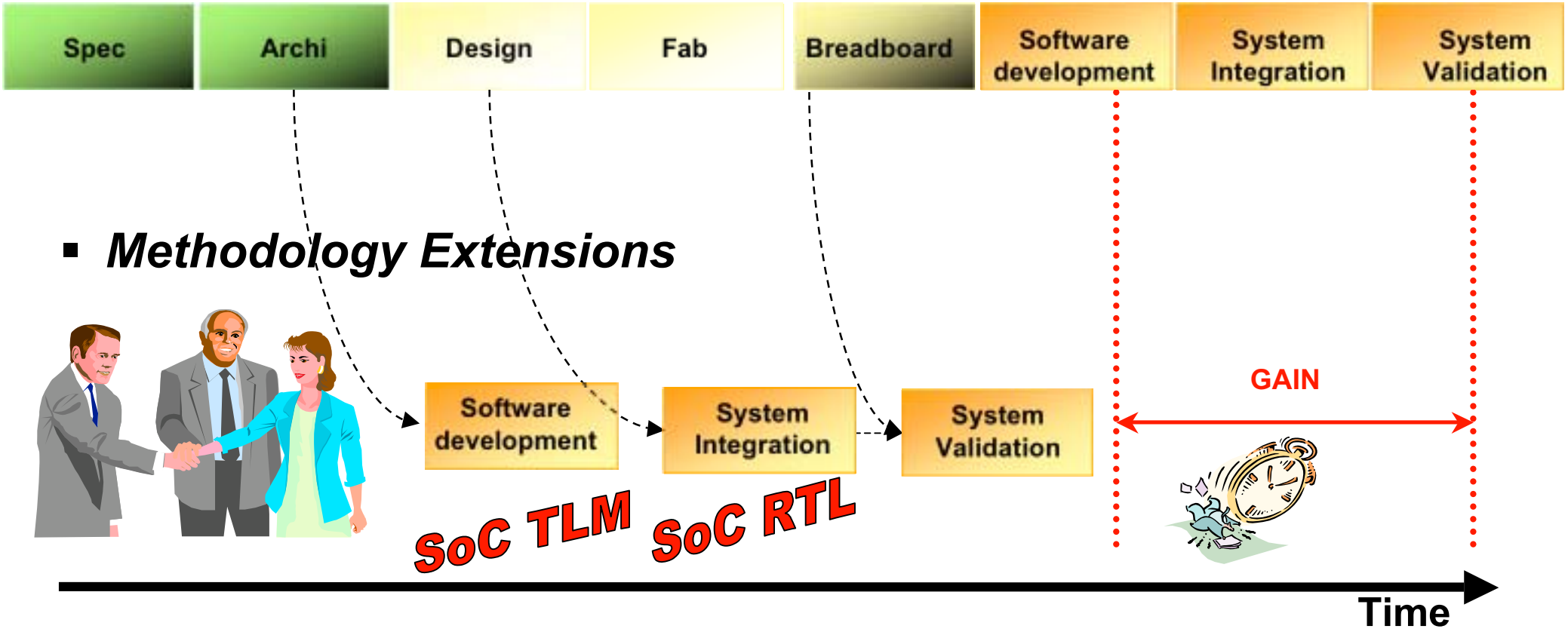
		0.13um	90nm
ST	Register files	spsmall	spsmall
			dpreg NEW
Partners		dprf	dprf
	High density	sphd	sphd
		dphd	dphd
		spuhd NEW	spuhd
	High speed	sphs	sphs
			spuhs NEW
		dphs	dphs
	High capacity	splarge	splarge
	Low Power	starsplp NEW	starsplp
			splp NEW
			dplp NEW
	rom	romv	romv
		romclp NEW	
	Multi port	mpa	multiport NEW
	CAM	bcam, tcam NEW	bcam, tcam
	Cache (data and tag)		spcache

Agenda

- Technology Evolution
- New system requirements
- Hardware/Software co-design
- Design Complexity and manufacturing costs
- Concurrent hard/software design and validation
- Flexible and Reconfigurable SoC
- Conclusion

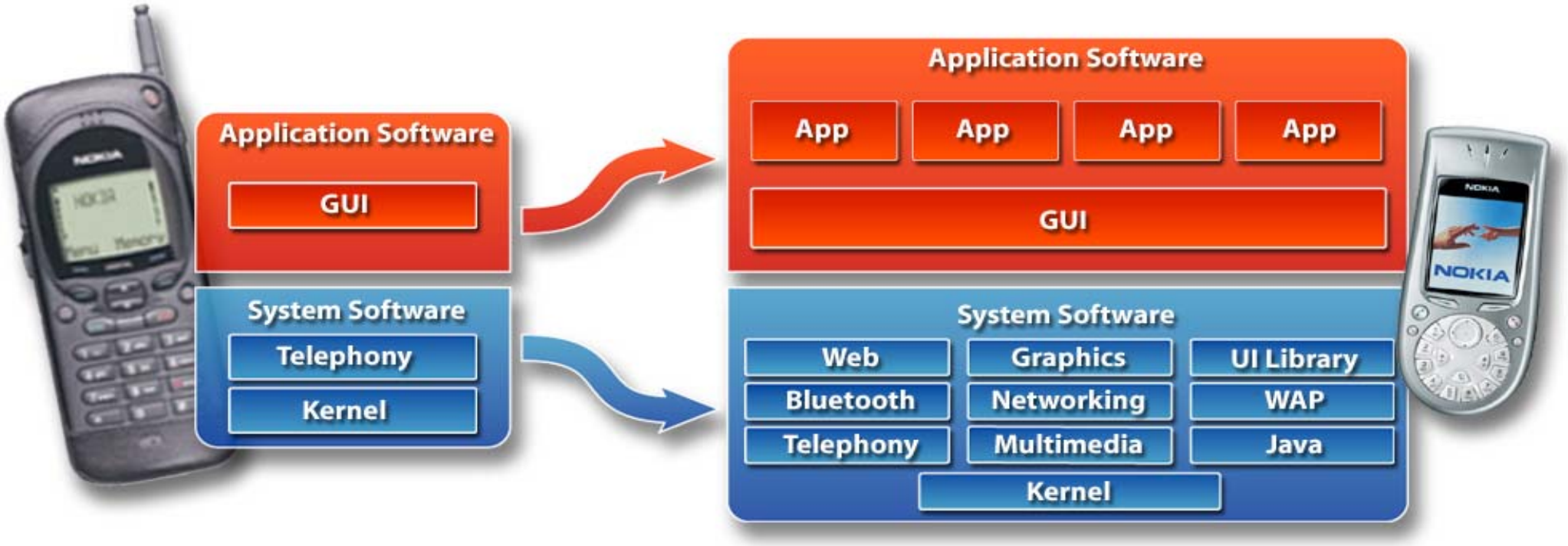
Concurrent Hardware/Software Design

- ***Standard Flow***



- ***Methodology Extensions***

Embedded Software Development Requires as Much/More Design Effort Than Hardware

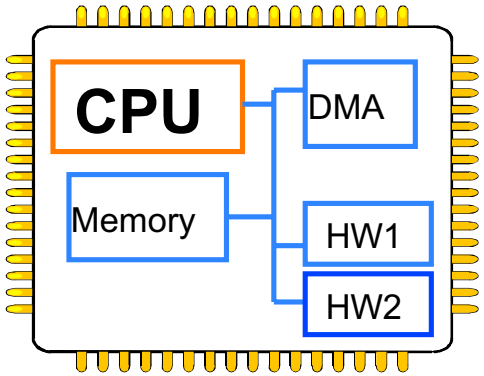


Operating-System is booting on simulated Cellphone (RTL)

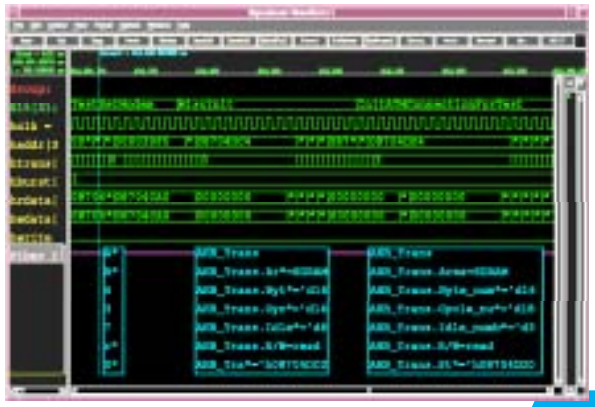
- ***Software***
  Real RTOS

  (Symbian)

Processor
ISS simu



Peripherals
RTL simulation



HW-SW Co-simulation
Cycle-Accurate
200 instr / sec

TLM models - Fast SoC simulations

Real embedded Software

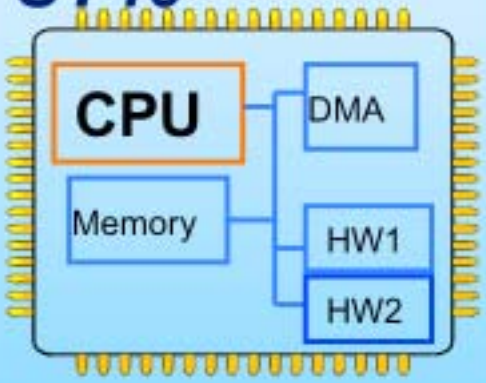
Application & Functional Verification

ST100 | SuperH | **ST20** | **ARM**

ST40

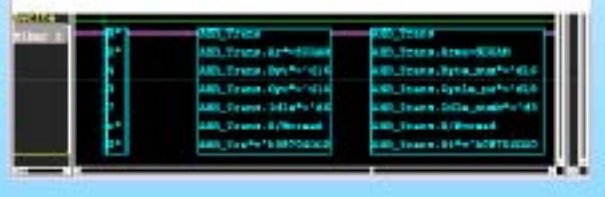
Processor

ISS simu



Peripherals

TLM simu



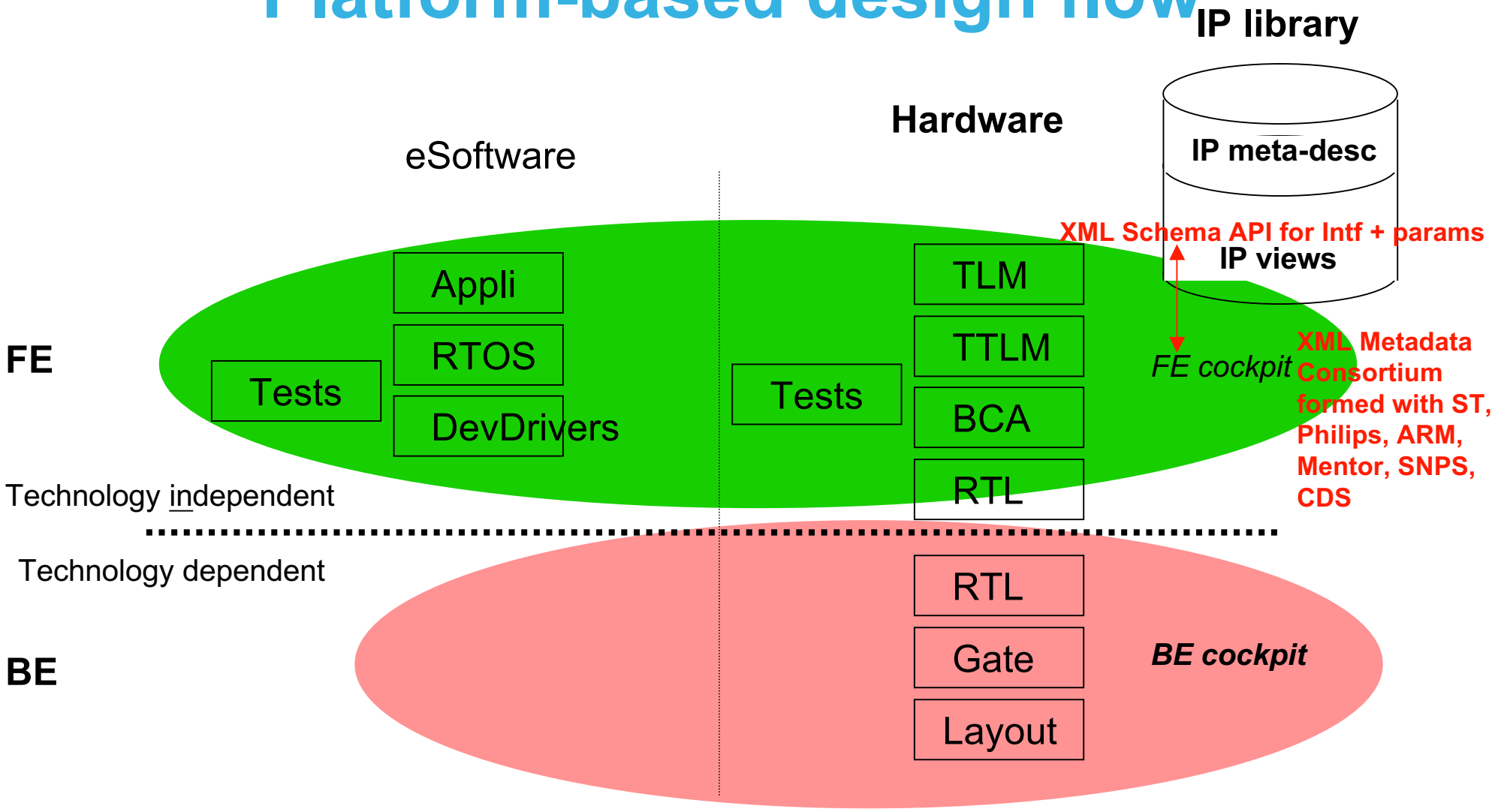
Standardization being proposed to SystemC OSCI by ST, Cadence, ARM

HW-SW Co-simulation

Transaction-Accurate

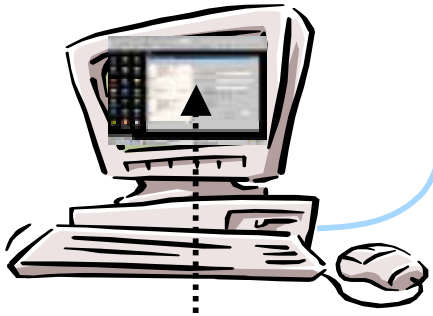
200 K+ instr / sec

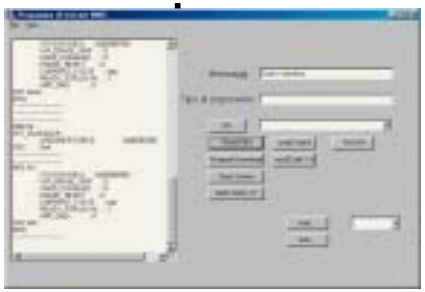
Platform-based design flow



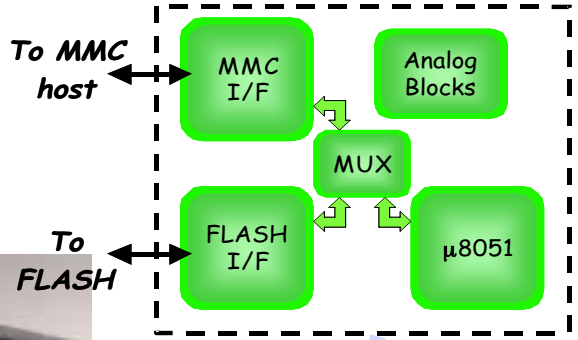
HW Emulation for MMC

- Real M58LW128 FLASH chip in-circuit





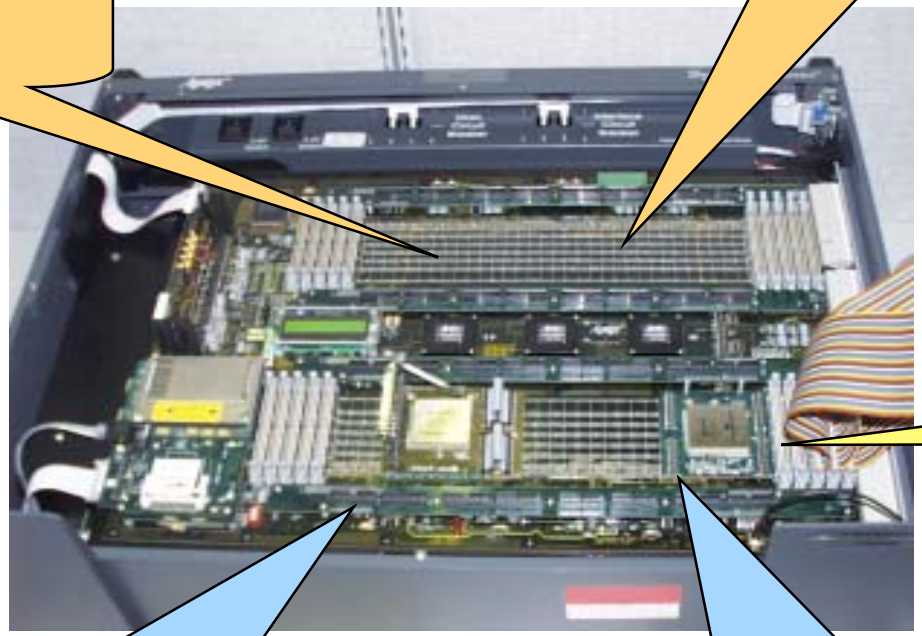
RTL Design



- 1w setup-time
- ~0.5MHz

- SW host running @100KHz
- Connection of HW host ongoing

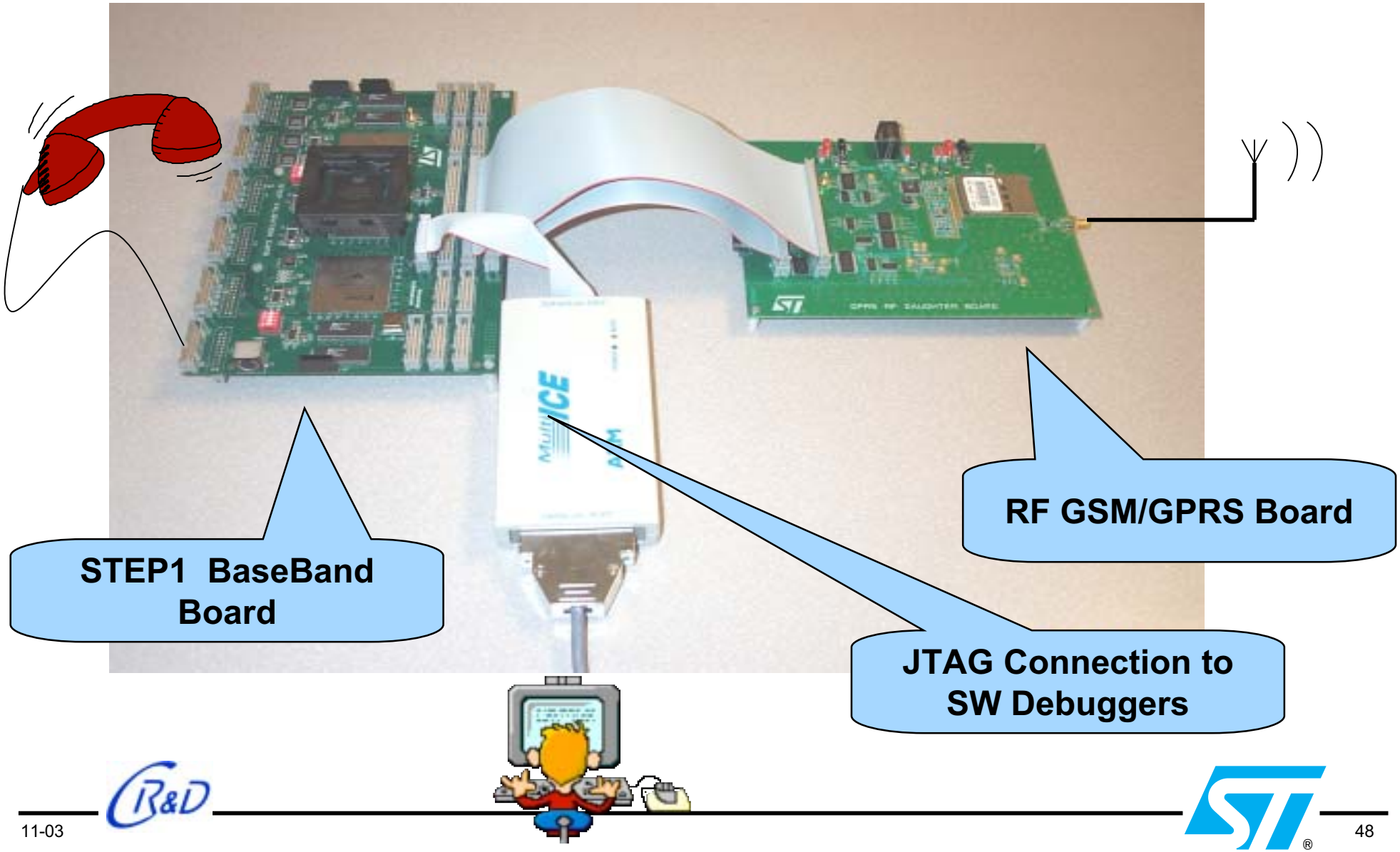
First Prototype Platform: Aptix



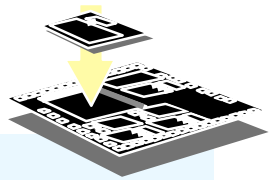
HW/SW fast prototype platform

- Faithful representation of the final design
- Available much sooner than the final silicon
- Guaranties the real-time behavior
- Validation of the fundamentals of the SoC HW/SW architecture

FPGA-based Prototyping Environment



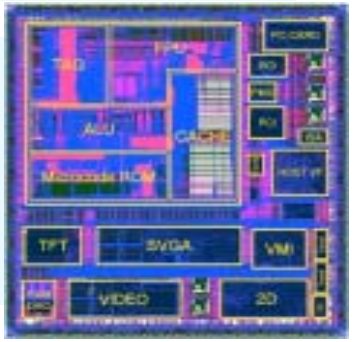
IP Reuse Program



- **Organization**
  - company program — "Design Methodology & IP Reuse", CEO sponsored
  - corporate driven — CR&D + cross-divisional Committee
  - domain-specific Work Groups — RTL2Layout, AMS, SLD, DFT, Functional Verif., Power, …
  - intranet information site — CAD On Line portal > K9 IP Reuse Pages

- **Reuse standards**
  - adherence to industry approach — VSIA; RMM; Quality
  - deliverables / views — BlueBook + Unicad Extension
  - IP packaging — bbview (mapping from BB logic views to IP physical files)
  - HDL coding style — Design Conventions + HAL associated checking tool
  - On Chip Bus — VCI-close STBus; AMBA

- **Methodology**
  - Development flow — Synopsys based Quartet
  - OCB support — STBus, AMBA Platform kits
  - System Level — SL model deliverables (TLM, BCA…)
  - Verification — dynamic, formal, H/W-S/W, integration



- **Infrastructure**
  - Design Data Manag[t]., Bug tracking — Products from Synchronicity, Rational
  - IP Quality (IP=Product) — IPScreen Certification; LibYield Maturity tracking
  - IP Procurement — IP On Line catalog; Procurement, Exchange procedures

IP certification
USB2.0 example

5 Summary

FS EBCV functional tests
PASS

HS EBCV functional
PASS

Device High-Speed sig

EL_2 PASS
EL_4 PASS
EL_6 PASS
EL_7 PASS

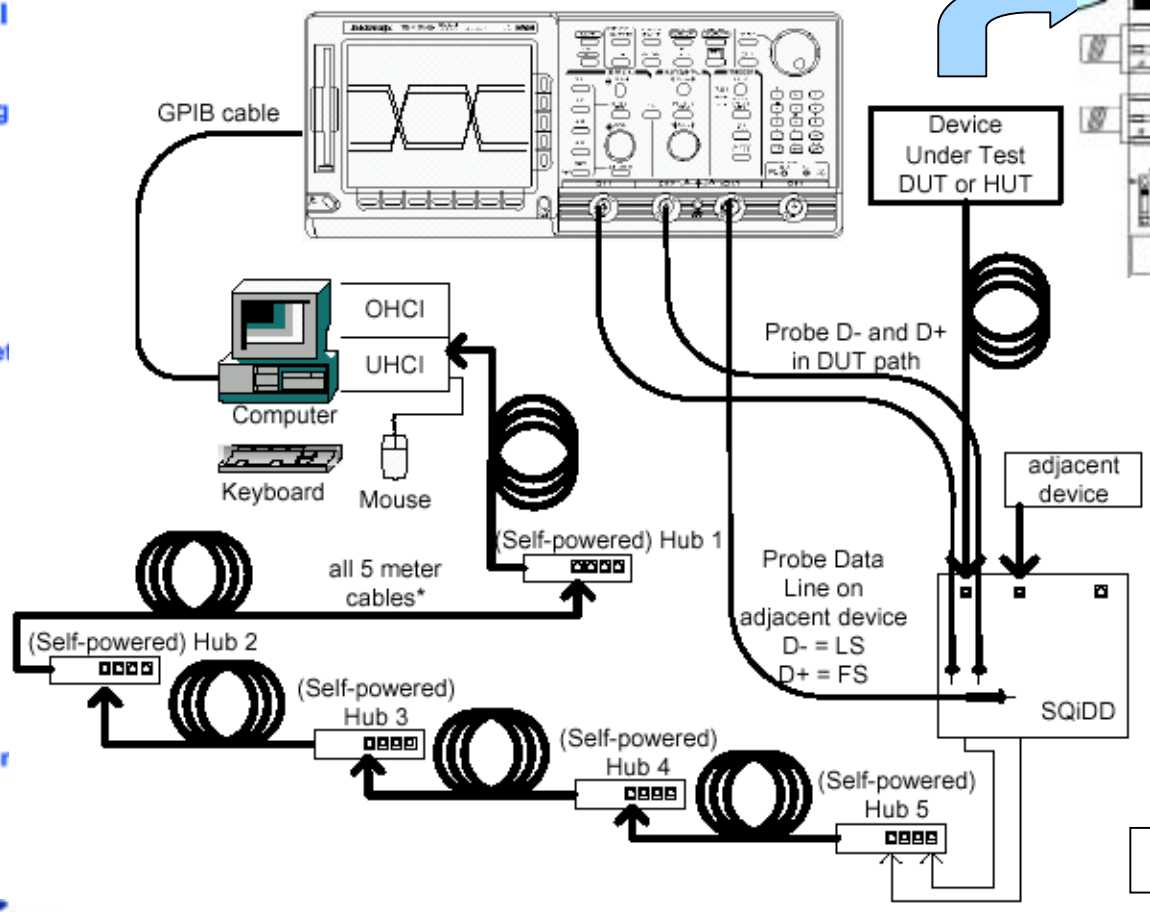
Device Packet Parame

EL_21 PASS
EL_22 PASS
EL_25 PASS

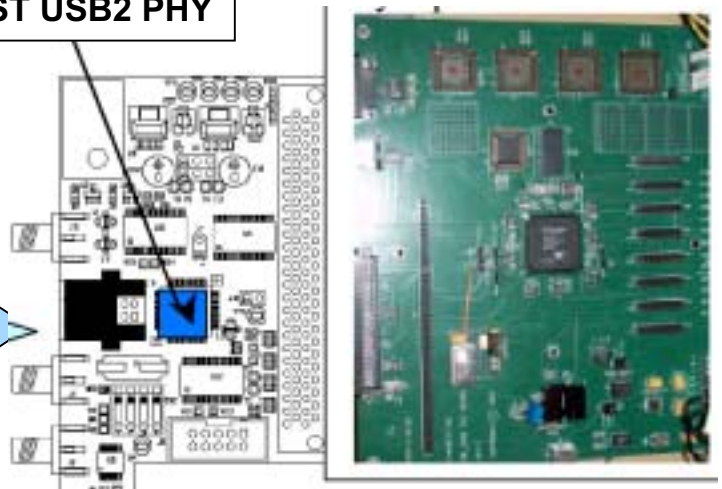
Device CHIRP Timing

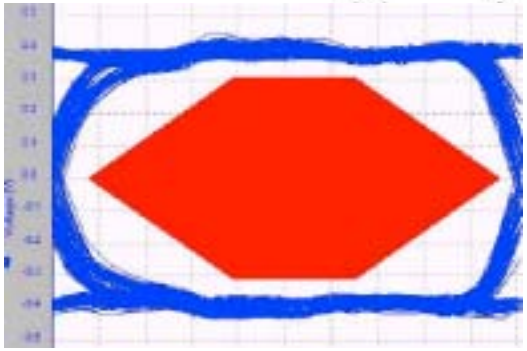
EL_28 PASS
EL_29 PASS
EL_31 PASS

Device Suspend/Resu



ST USB2 PHY

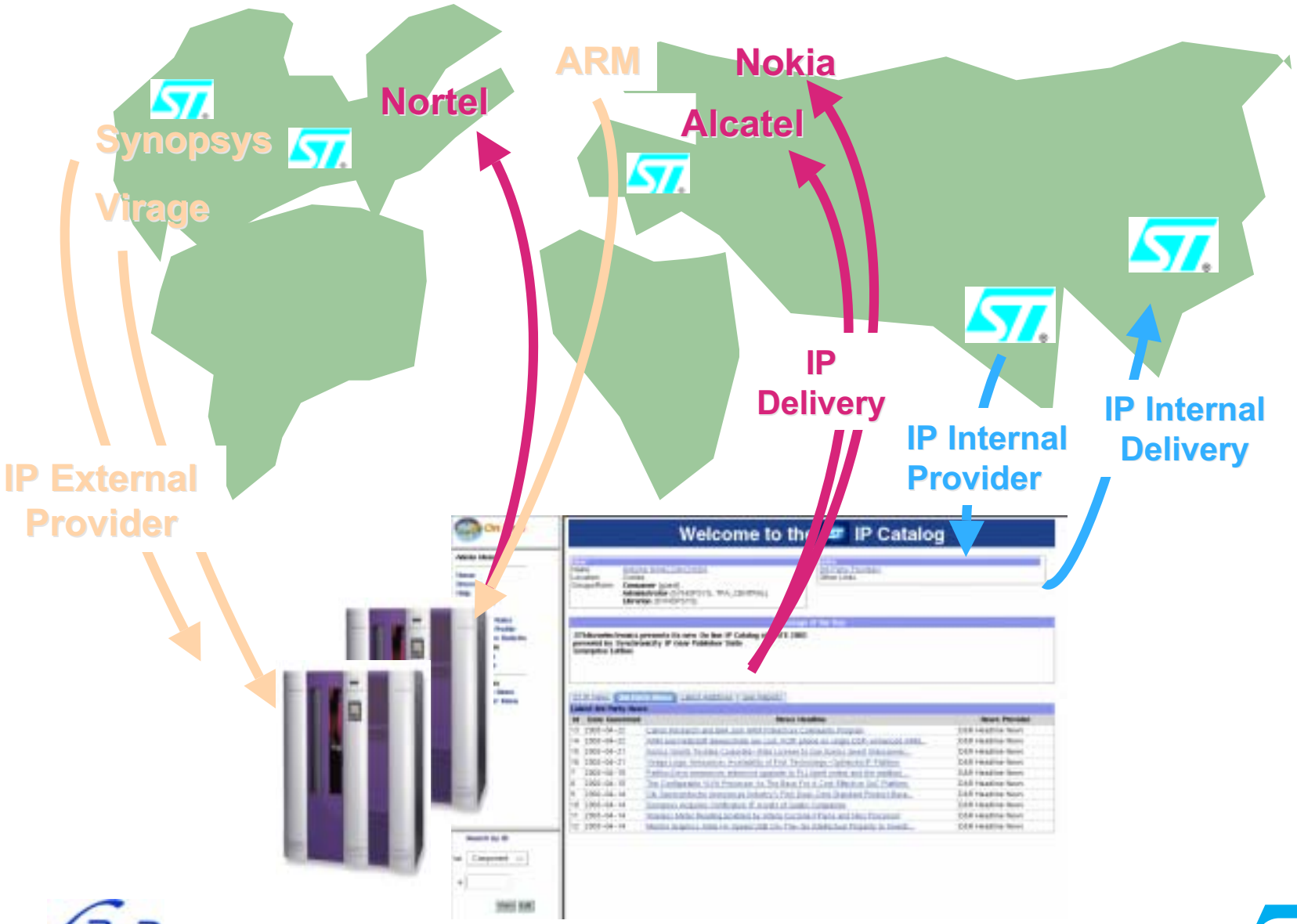




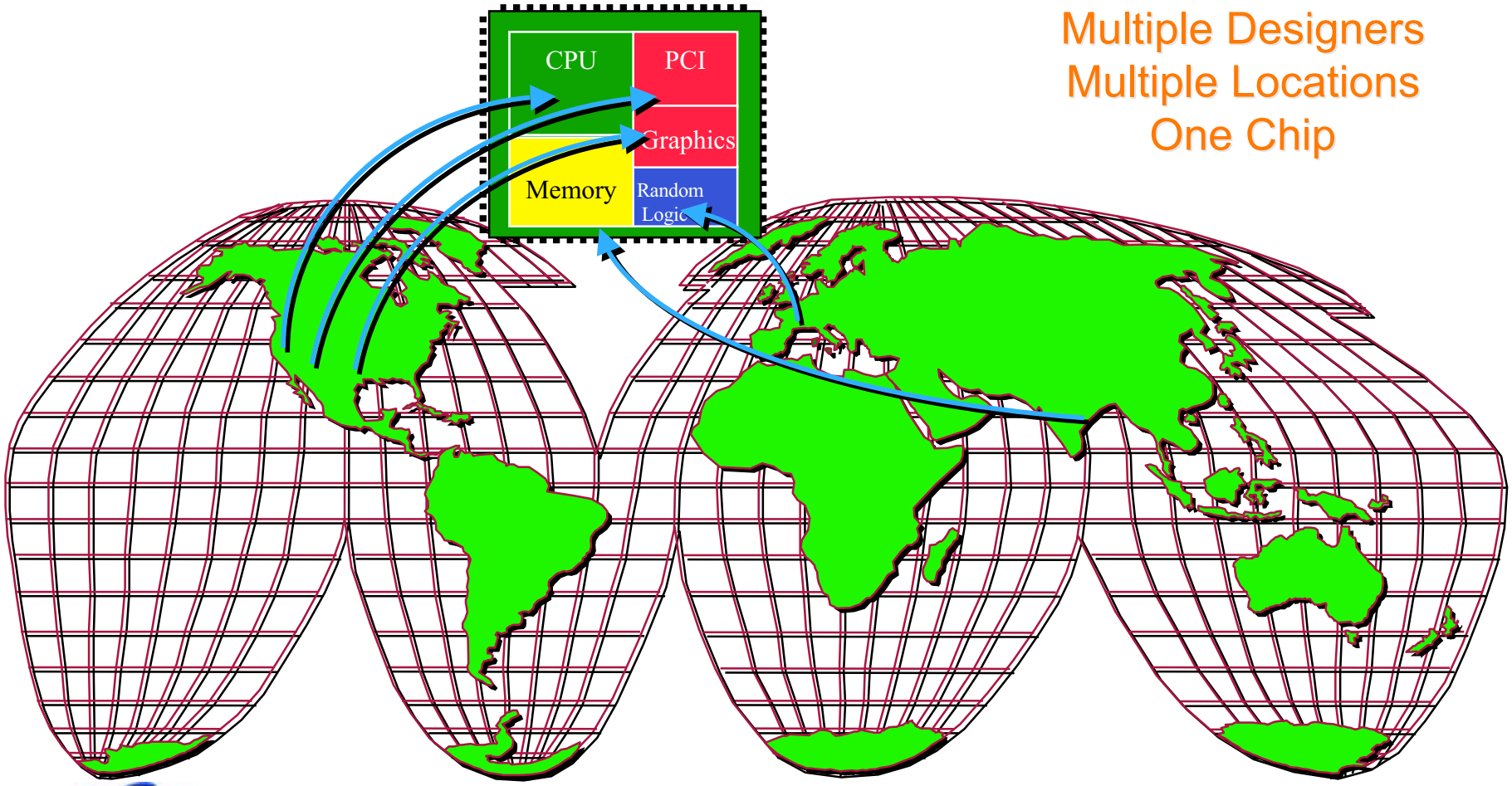
HI-SPEED CERTIFIED USB

If you pass OK, you have the logo

Corporate IP Catalog Project



Multi-Site Collaborative Design (Synchronicity-based)



Multiple Designers
Multiple Locations
One Chip